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TECHNICAL NOTE TN6-1

FDC 9216 FLOPPY DISK DATA SEPARATOR

1. INTRODUCTION

Data written to a floppy disk drive is typically a self-clocking encoded serial data stream. Two methods of encoding are in widespread use today: Single-density recording, also known as FM (Frequency Modulation) and Double-density recording, also known as MFM (Modified Frequency Modulation).

The function of a data separator is to derive a clock signal from the combined clock/data waveform available from the output of most disk drives. This clock signal should be one suitable for input to one of the popular disk controllers such as the SMC FDC 179X family or the NEC 765 controller.

A typical FM encoded signal is shown in Figure 1A and a typical MFM encoded waveform is shown in Figure 1B. The clock signals or windows required for the floppy controllers are also shown in the figures. Note that the clock signal is really a signal which is used to delineate the half-bit slots in the disk data separator waveform to allow the controller to separate clock slots from data slots.

One scheme for data separation is shown in Figure 2A. The disk data is presented directly to the controller and the data separator provides a derived clock to define the half-bit slots. Most analog phase-locked loop data separators are connected in this way. Figure 2B shows another scheme for data separation. The disk data is remembered by the data separator and regenerated for presentation to the disk controller. The derived clock is also regenerated to maintain proper synchronization with the regenerated data. The FDC9216/B is a floppy disk data separator of this type.

Figure 3 shows the single and double density waveforms used to represent the eight-bit byte "D1" (hexadecimal) in floppy disk systems. Each of the eight bit times, b0 through b7, is comprised of a clock half-bit slot followed by a data half-bit slot. Data is represented by a pulse within the data slot for a one, and by the absence of a pulse within the data slot for a zero.

The purpose of the clock slots is to provide positions for the insertion of non-data pulses in the waveform which help the data recovery hardware keep accurate count of bit times. Without pulses in the clock slots, the representation of an all-zero data byte would be a featureless waveform eight bit times long. It would be difficult for the data recovery hardware to know how many bits of zero had been received especially with variations in disk speed.

Rules for single-density encoding require a pulse to be inserted in each clock slot. This is shown in waveform B of Figure 3. Double density rules specify pulse insertion in clock slots only between consecutive zeros as shown in waveform A. Since the controller determines whether a half-bit slot is a clock slot or a data slot, the data separator is able to treat clock slots and data slots identically. This is fortunate since radically different data patterns can have nearly identical double density representations, as shown in Figure 4. It is the responsibility of the data separator to separate the data waveform into half-bit slots by providing an accompanying clock waveform, but it is the responsibility of the controller to differentiate clock slots from data slots. (This is usually done by the use of special bytes which "break the rules" regarding clock slot pulse insertion, making them distinguishable from ordinary data bytes).

2. THEORY OF OPERATION

Figure 5 shows the relationship of the clock waveform to the half-bit slots required by several currently available floppy disk controllers. The end of one half-bit slot and the beginning of the next is defined by a transition of the clock waveform. Both positive-going and negative-going transitions are handled identically, and the fact that the clock waveform is high during one half-bit slot and low during the next is of no importance in differentiating clock slots from data slots. Thus, clock waveforms A and B in Figure 5 are functionally identical.

The position of a pulse in the data waveform is taken to be its leading edge. Thus, as shown in the ideal data waveform of Figure 5, the leading edge of each pulse should be centered in its half-bit slot, midway between clock waveform transitions. If a pulse is widened so that the clock waveform transitions during the pulse, the pulse is still associated with the half-bit slot containing the leading edge.

Figure 5 also shows a distorted data waveform, more realistic than the ideal data waveform. Magnetic effects on the disk (mainly peak shift as shown in Figure 6) cause pulse positions to vary from ideal, as do variations in disk speed. As a result, many pulses occur early or late within their half-bit slots. It is therefore important that the derived clock delineate the half-bit slots as accurately as possible so that the position of a pulse may vary with the greatest margin and still be associated with the correct half-bit slot. This is accomplished by adjusting the phase of the derived clock so that the average position of the last several pulses is centered in the half-bit slot.

The heart of the FDC9216/B Floppy Disk Data Separator is a synthetic oscillator phase-locked loop. One half-bit slot of the incoming data stream corresponds to one cycle of the synthetic oscillator. Each oscillator cycle consists nominally of eight phase slices, identified in Figure 7 as phase memory values 1 through 8. The circuit therefore needs a phase slice clock with a frequency eight times the half-bit frequency.

Detection of an input pulse away from the center of its half-bit slot (in other than phases 4 or 5) causes a phase correction to be applied to the synthetic oscillator, bringing the center of the half-bit slot closer to the pulse. Referring to Figure 7, input pulse 'A' in slot 1 is centered, so no correction is applied. Input pulse 'B' in slot 2 is early, so the slot is shortened by skipping phase 3. Slot 3 contains no input pulse and is not corrected. Input pulse 'C' in slot 4 is late, so the slot is lengthened by repeating phase 8.

The end-of-cycle signal from the internal synthetic oscillator phase-locked loop logic function array defines the derived clock waveform and the duration of each half-bit slot. The occurrence of an input detection during the half-bit slot is remembered and used to regenerate the data waveform pulses immediately following end-of-cycle. The relationship between detected and regenerated pulses 'A', 'B', and 'C' is shown in Figure 7. A delayed form of end-of-cycle is used to toggle the regenerated clock so that the regenerated data pulses are more nearly centered with respect to the regenerated clock (for compatibility with existing controllers).

The variation in the rotational speed of many floppy disk drives is as much as two percent. If data is recorded on a drive running two percent slow, and retrieved on a drive running two percent fast, the disk data waveform presented to the data separator will be four percent faster than nominal. Similarly, the data separator may also be required to

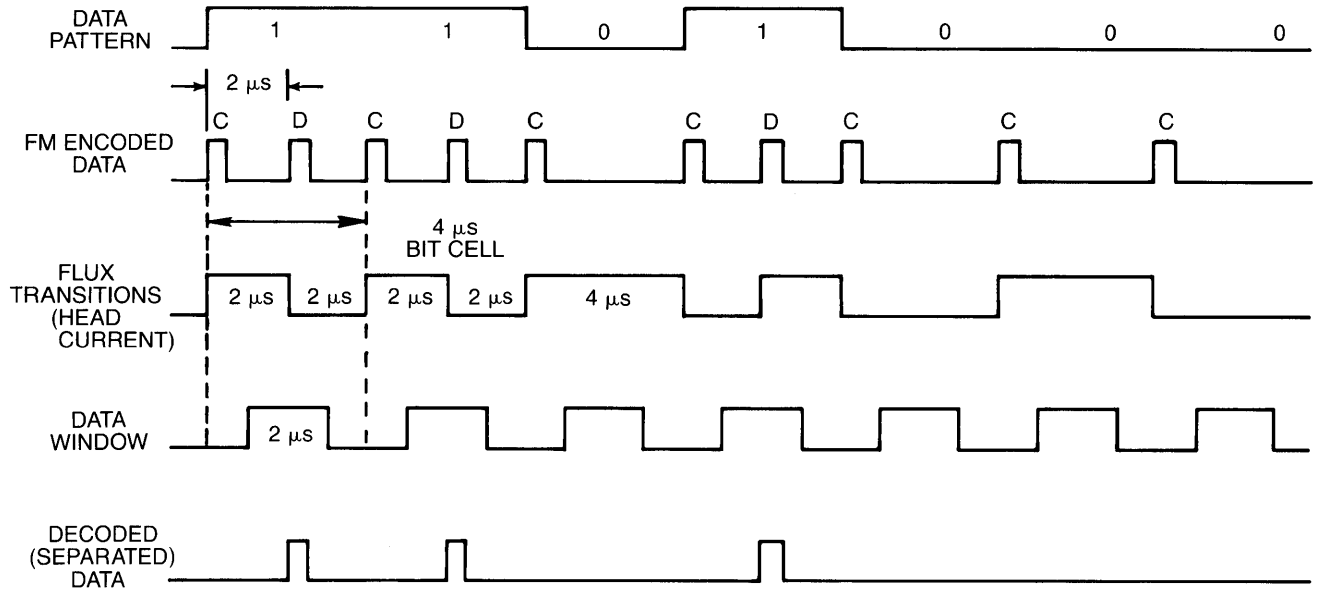


FIGURE 1A: FM ENCODING SCHEME

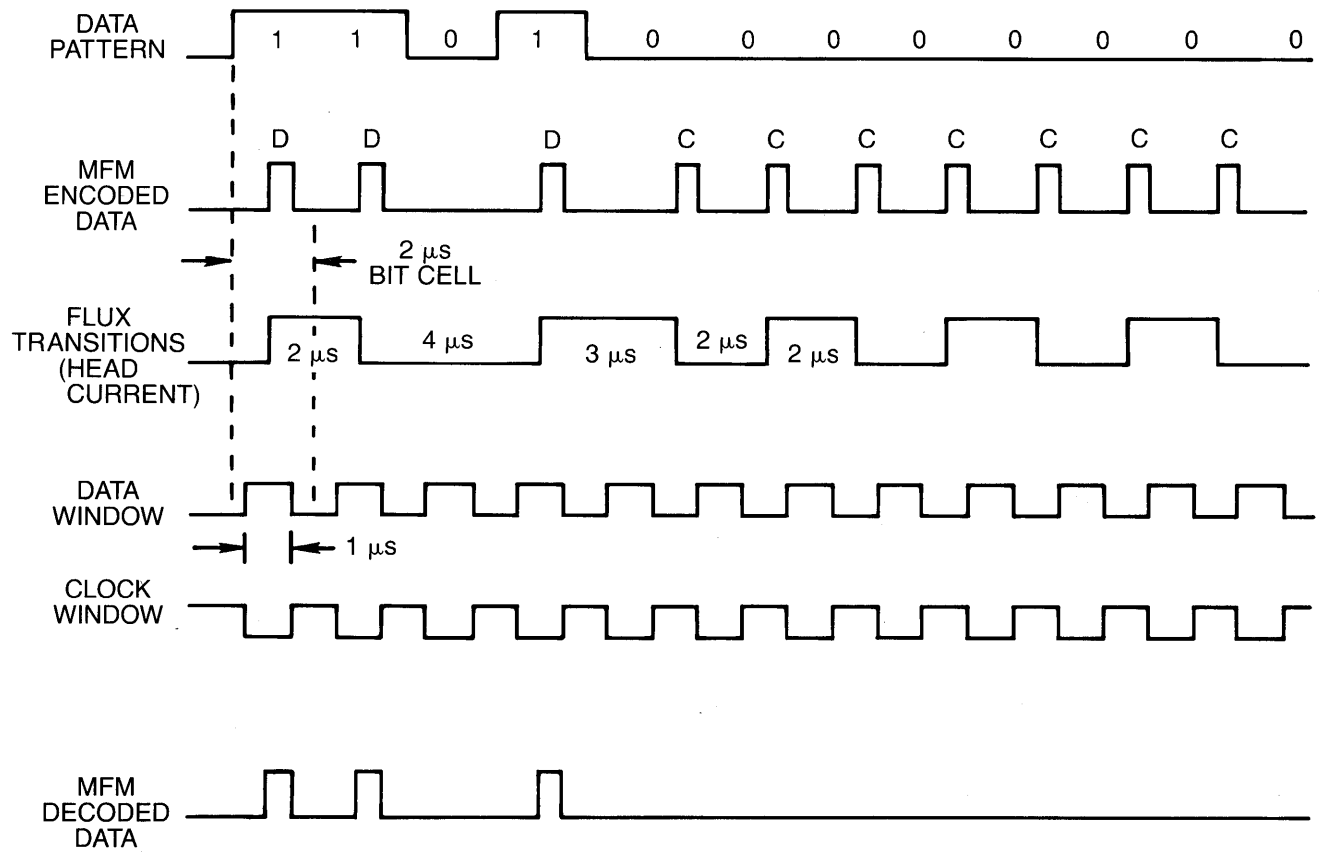


FIGURE 1B: MFM ENCODING SCHEME

handle incoming disk data as much as four percent slow. To compensate for these variations in average half-bit frequency, center-frequency correction is added as an improvement to the synthetic oscillator phase-locked loop algorithm. A short history is kept of input pulse detections which induce phase corrections. This history is used to allow subsequent phase corrections to request upward or downward changes in center frequency.

3. TYPICAL SYSTEM CONFIGURATION

Figure 8A shows a system configuration using the FDC179X Floppy Disk Formatter Controller and the FDC9216/B Floppy Disk Data Separator. Figure 8B shows a system configuration using the NEC 765 Floppy Disk Controller and the FDC9216/B Floppy Disk Data Separator.

Note that a write precompensation circuit is also included. Write precompensation is typically performed on the write data to reduce the amount of peak shift in the recovered data. Since peak shift is data pattern sensitive, its direction can be predicted by the Floppy Disk Controller/Formatter. This information is used when writing the data on the disk to cause particular flux transitions (or pulses) to be written early or late from their nominal positions. This causes the recovered data to appear closer to its nominal bit position.

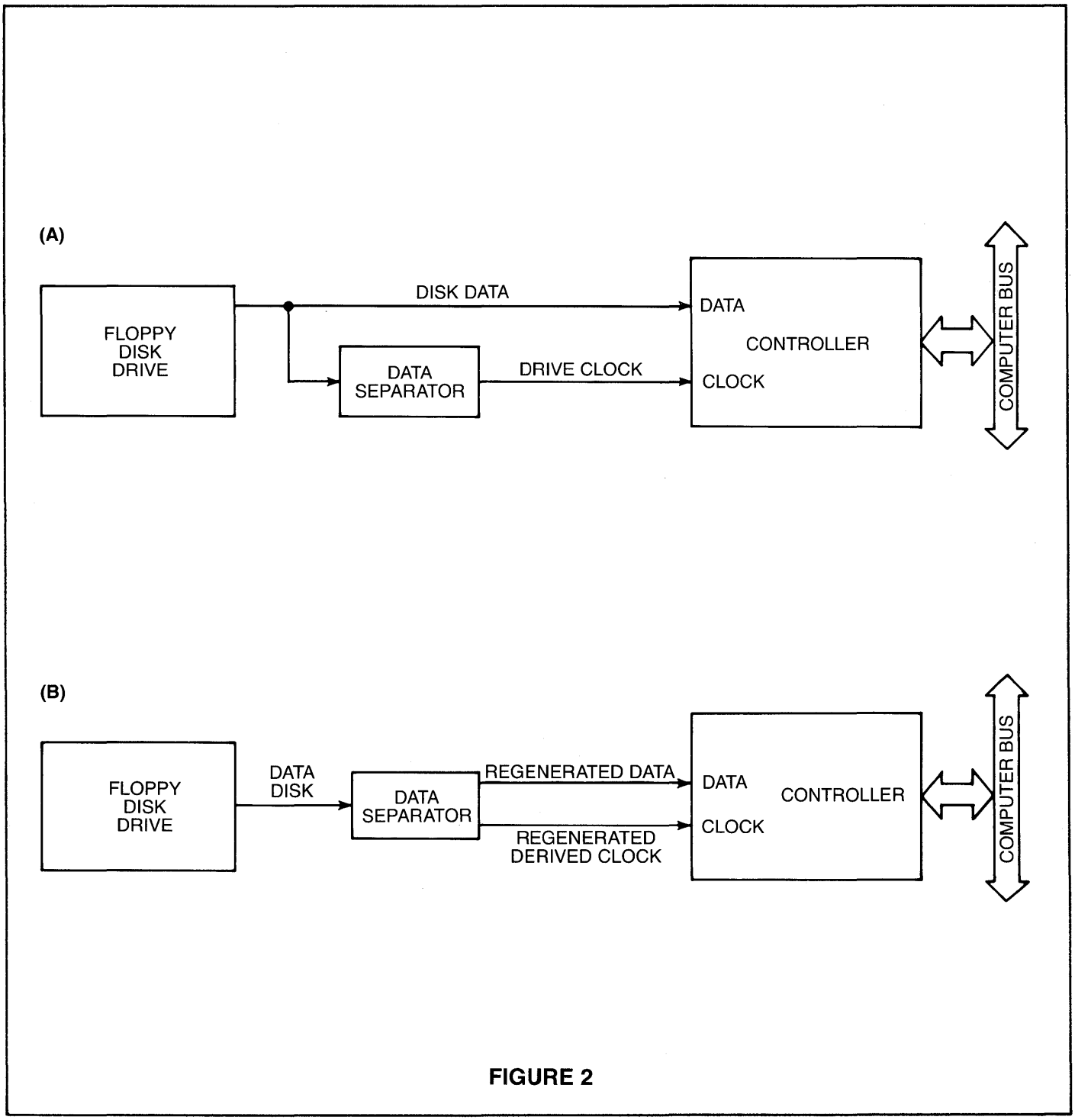


FIGURE 2

4. CHARACTERIZATION TEST RESULTS FOR 5¼" DRIVES

The FDC9216/B has been tested for error performance with a variety of 5¼" floppy disk drives. During the tests it was found that the performance of the FDC9216/B is enhanced by the selection of an optimum value of write precompensation for the particular type of drive being used. The object of the tests were as follows:

1) To determine the optimum write precompensation for each manufacturer's drive type.
2) To determine the overall error rate of each drive type at nominal speed.
3) To determine the error rate of each type of drive over a speed variation range of plus or minus 2% from nominal. This typifies the worst case for a disk that is written on one drive and read on another.
4) To determine the overall error rate of the FDC9216/B over all drives tested at nominal speed and at plus or minus 2% speed variation.

The following test configuration and drives were used:

Test Configuration:

Test System —North Star S100 System with SMC FDCS100 disk controller board operating the drive under test.

Test Program —DISKSCAN test program, for use with the FDCS100 board.

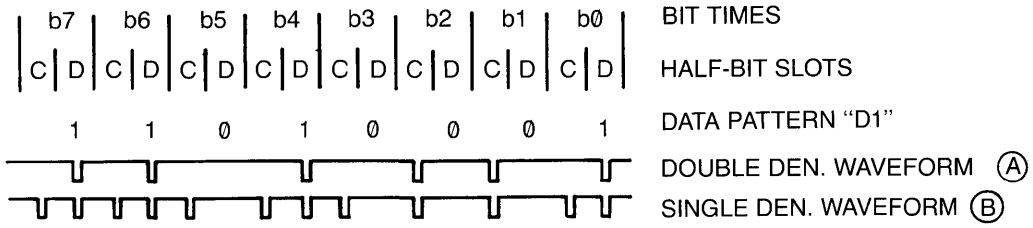


FIGURE 3

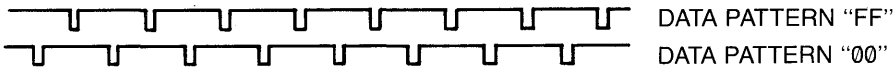


FIGURE 4

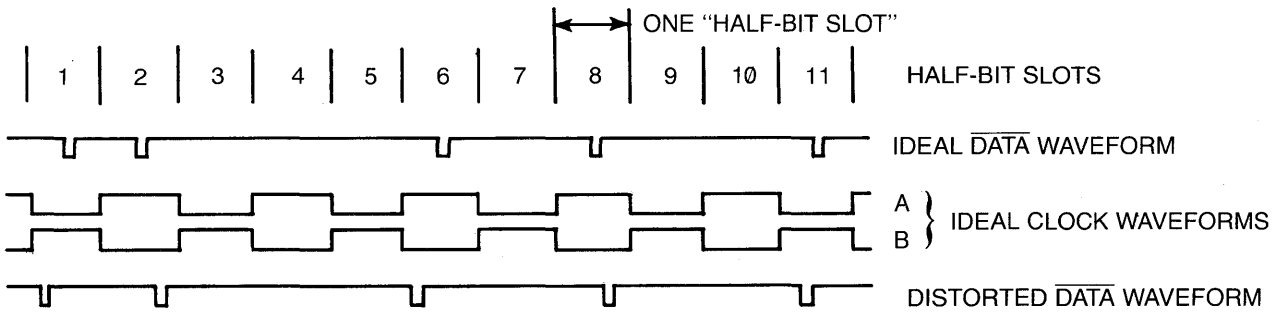


FIGURE 5

Media — 1. Structured Systems Group, 5¼", single-sided.
2. Maxell, 5¼", single-sided, MD1.
3. Maxell, 8", single-sided, FD1.
4. Dysan, 5¼", 104/2D.

Drives: — 1. Magnetic Peripherals, 5¼", Model 9408, Serial Number 001298
2. Shugart Assc., 5¼", Model 400, Serial Number B001160
3. Qume, 5¼", Model DT/5, Serial Number 19516
4. Tandon, 5¼" Model TM100-1A, Serial Number 81380111
5. Qume, 5¼", Model DT/5, Serial Number 60475
6. Shugart Assc., 5¼", Model 400, Serial Number L12492
7. Shugart Assc., 5¼", Model 410, Serial Number A13183
11. Micro Peripherals, 5¼", Model 51S, Serial Number 123487

The media used were standard off-the-shelf Maxell, Structured-Systems, and Dysan single-sided flexible disks. The entire disk was written with a double-density MFM data pattern of 256 "6D" (hex) bytes in each sector. This pattern was chosen because it contains the worst-case bit-shift patterns. Each individual test consisted of 1.0E9 bits read and was accomplished by repetitively reading the disk. (Note: The notation "E9" should be read as "times 10 to the ninth power")

Figure 9 shows the results of the write precompensation tests for each drive. Each dot in each graph represents the actual error rate for 1E9 bits formatted and read at the indicated precompensation value at nominal speed. For each test write precompensation was applied uniformly to all tracks. For all drives there was at least one value of precompensation, and in most cases several values, which produced zero errors in 1E9 bits written and read back at nominal drive speed. Note that some drives have a much wider variation in write precompensation range than others.

Overall, these tests indicated that a write precompensation value in the range of 250 to 438ns is suitable for most 5¼" drives. The speed variation tests are, of course, more stringent. For each drive this test consisted of reading in excess of 1.0E9 bits with the data written on the drive running 2% slower than nominal, then read back on the drive set to run 2% faster than nominal. This had been determined to be the worst case speed test for the FDC9216/B. For each drive the results were as shown in Table 1.

Drive #	Speed Variation Soft Error Rate	Precompensation @ (ns)	Remarks
1	<1 in 1.0E9 bits	250	
2	1 in 2.0E8 bits	375	
3	1 in 1.0E9 bits	438	
4	1 in 1.0E9 bits	250	
5	1 in 5.0E8 bits	438	
6	<1 in 1.0E9 bits	375	
7	1 in 1.0E9 bits	312	
11	1 in 1.4E8 bits	438	

TABLE 1

All read errors were "soft" errors, that is the data was completely recovered when the sector was read again on a subsequent pass. Based on the speed variation tests above, the overall worst case error rate was one error in 4.7E8 bits read. It should be noted that drives 1 and 6 had no errors at all at the time the test was terminated after 1.0E9 bits read.

5. CHARACTERIZATION TEST RESULTS FOR 8" DRIVES

A number of tests were performed on 8" drives. The following four drives were tested:

Drives — 8. Shugart Assc., 8", Model 800, SNK59696
9. Shugart Assc., 8", Model 800, SNB77977
12. Qume, 8", Model Qumetrak 842, SN114079
13. Tandon, 8", Model TM848, SN006293

Figure 10 shows the results of the write precompensation tests for these drives. For these drives a value of 187 to 312ns was optimal. For drives 8, 9, and 13, write precompensation was applied only on track positions greater than 43. However, drive 12 produced the lowest error rate when write precompensation was applied to track positions greater than 27. The speed variation tests consisted of writing the data at a 4% faster rate and reading it back at nominal speed. All read errors were "soft" errors. The results are shown in Table 2.

Drive #	Speed Variation Soft Error Rate	Precompensation @ (ns)	Remarks
8	<1 in 1.0E9 bits	312	Also <1 in 1.0E9 bits @ 4% recorded slow, played back nominal.
9	1 in 1.0E9 bits	250	
12	1 in 5.0E8 bits	312	Precomp applied to tracks greater than 27.
13	1 in 1.0E9 bits	187	

TABLE 2

6. SUMMARY

These tests indicate that the FDC9216/B is an extremely effective data separator. The error rates are acceptable for virtually all systems. Further, all errors were soft errors which were subsequently re-read without error. Furthermore, the observed error rates were system error rates; that is, the entire system including disk drive, data separator, floppy disk controller, power supply etc. all contributed to the resultant error rate. The data separator does not stand isolated but is rather one of several elements in the data recovery process. Its low-cost, absence of finicky user adjustments (pots), and small-size make the 8-pin FDC9216/B ideal for most floppy disk system applications.

PEAK-SHIFT EFFECTS

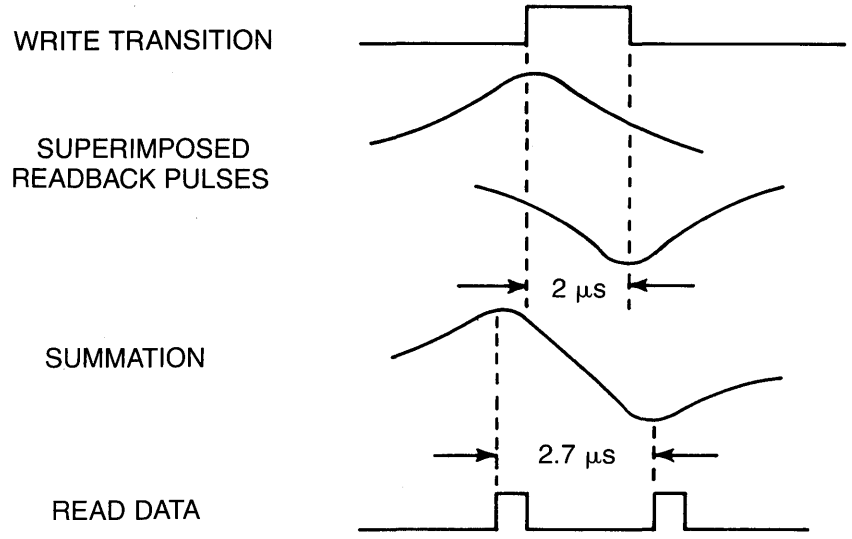


FIGURE 6

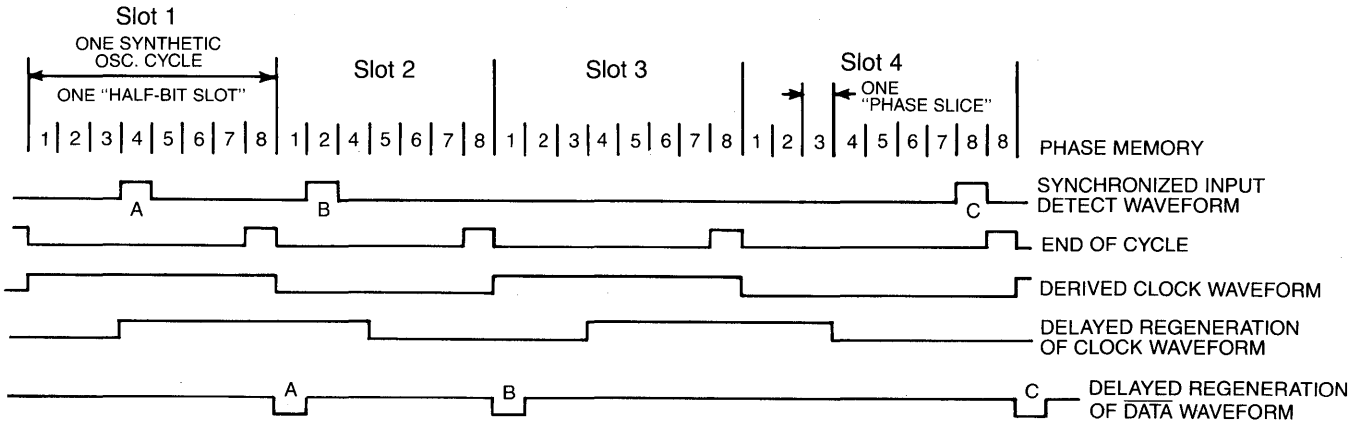


FIGURE 7

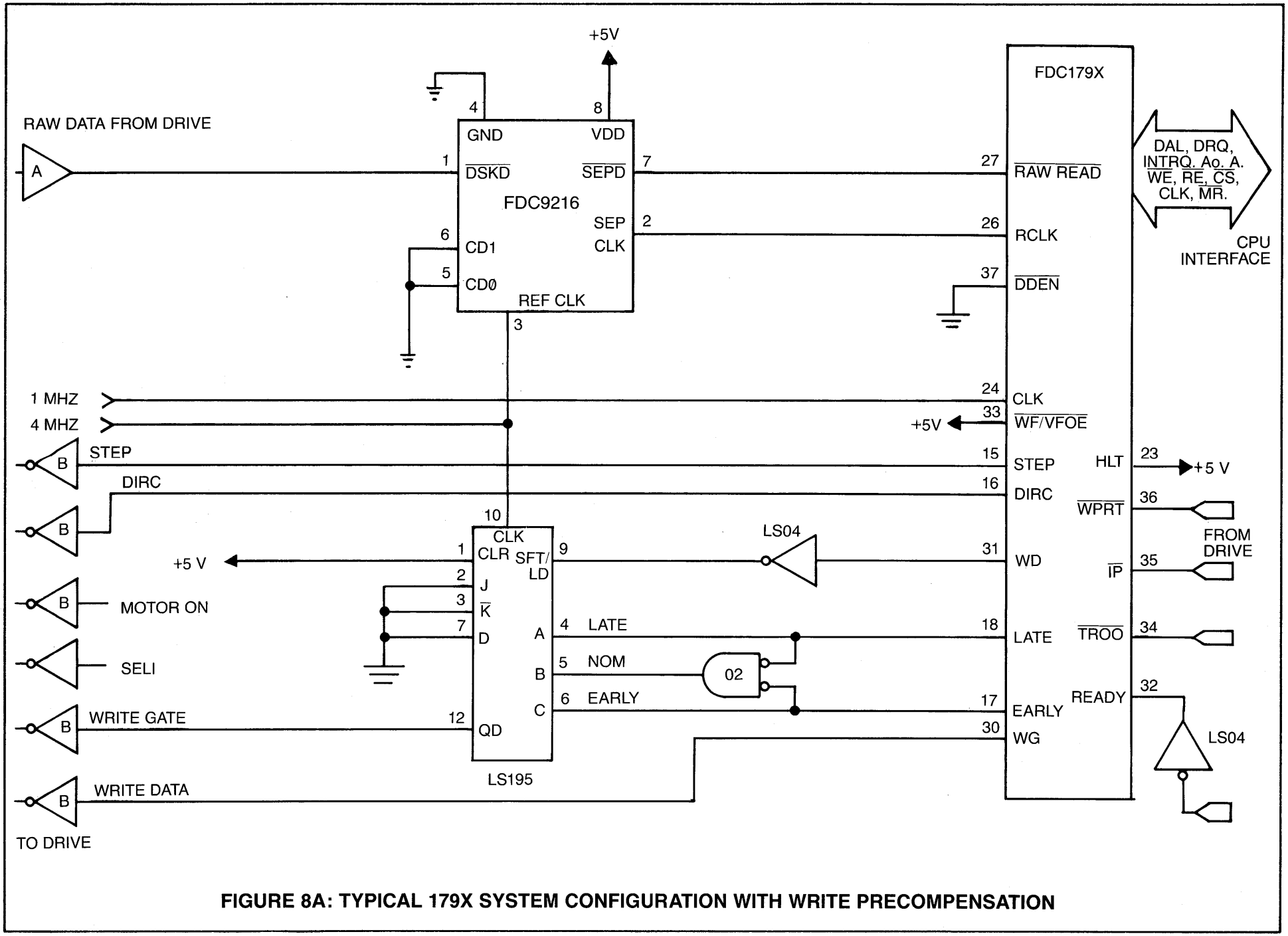
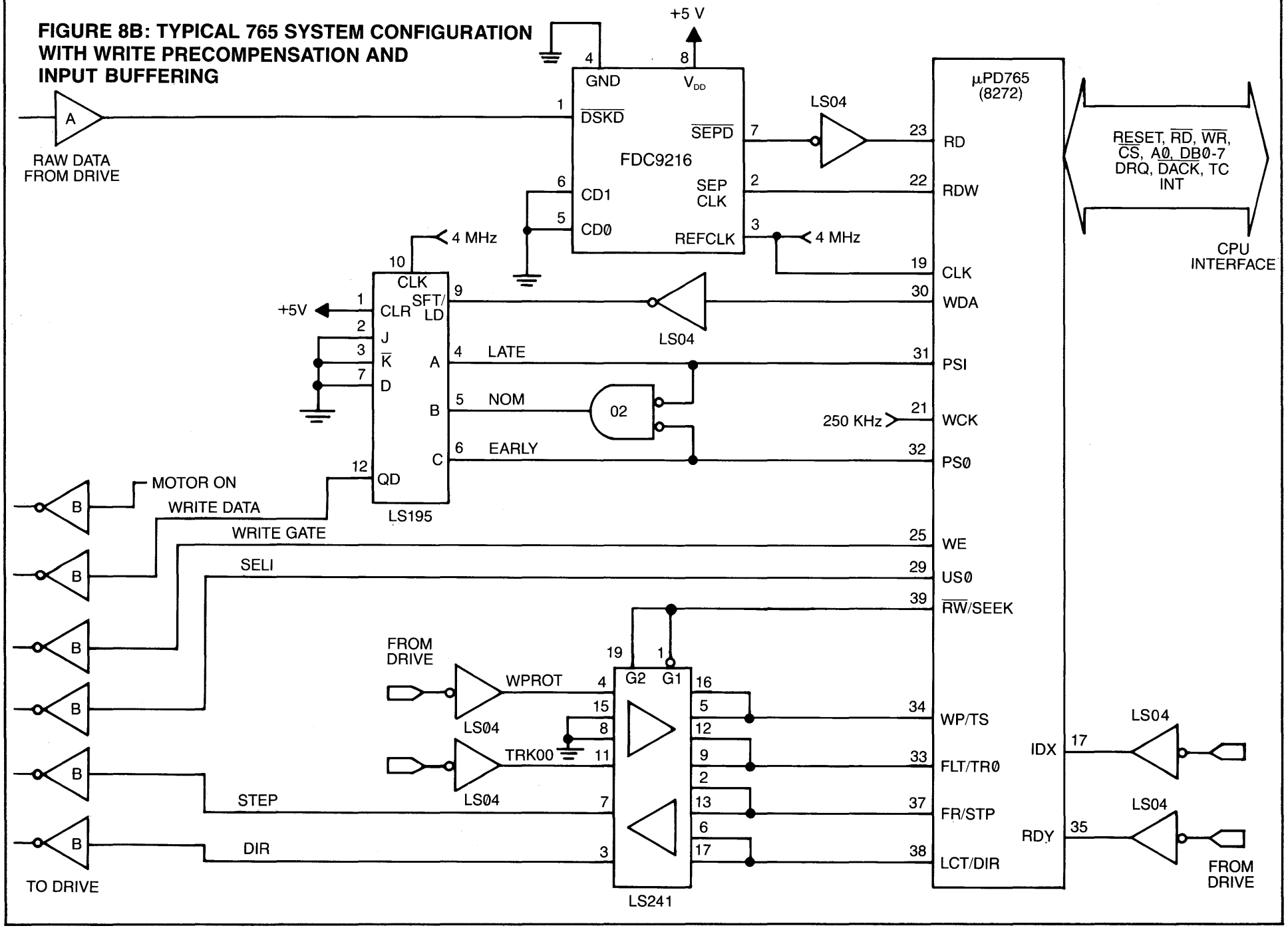


FIGURE 8A: TYPICAL 179X SYSTEM CONFIGURATION WITH WRITE PRECOMPENSATION

FIGURE 8B: TYPICAL 765 SYSTEM CONFIGURATION WITH WRITE PRECOMPENSATION AND INPUT BUFFERING



PRECOMP TEST

V SCALE = NO. OF BITS READ/1 ERROR.
H SCALE = AMOUNT OF PRECOMP USED TO FORMAT TRACK.

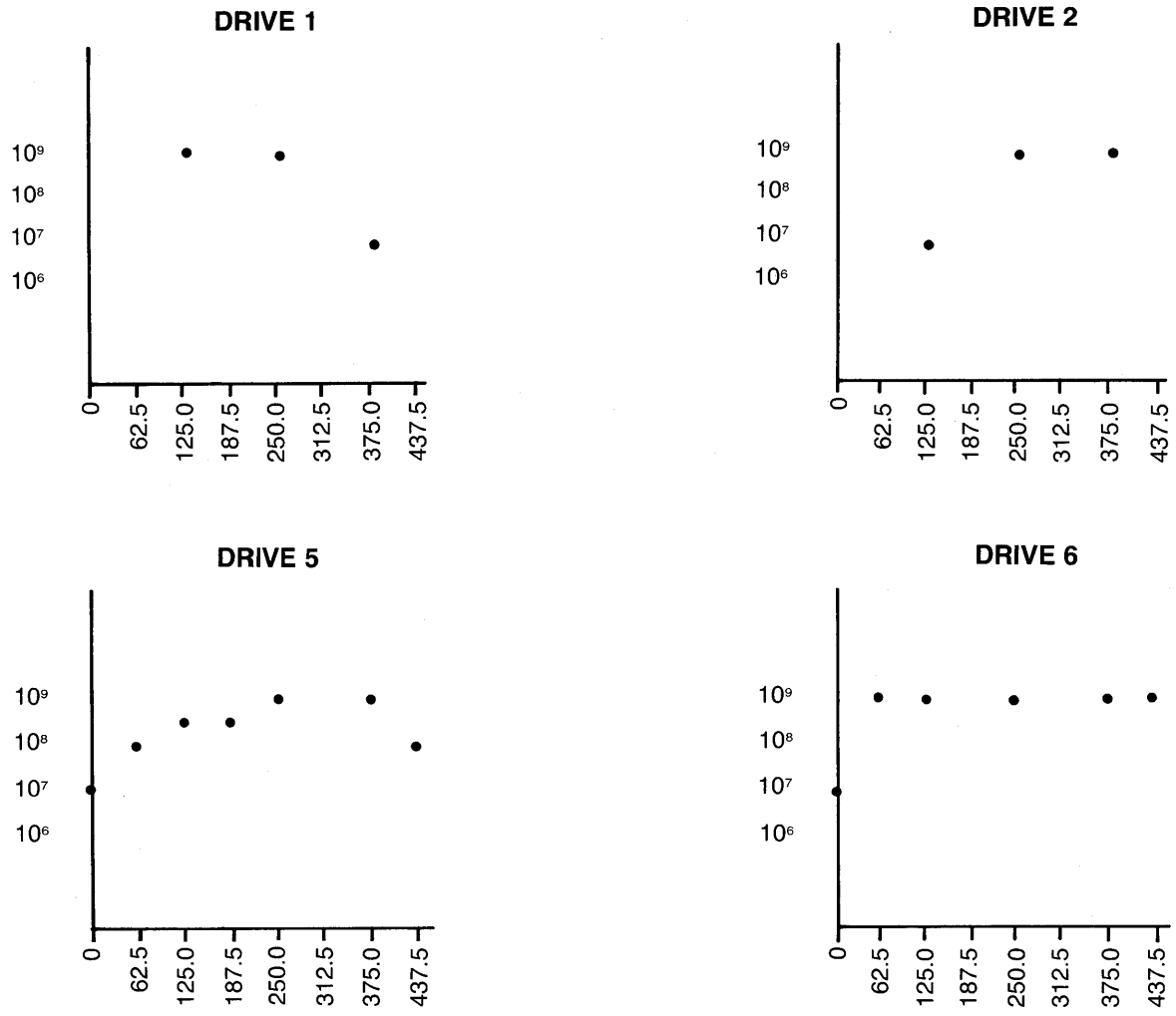


FIGURE 9: 5¼″ DRIVE WRITE PRECOMPENSATION

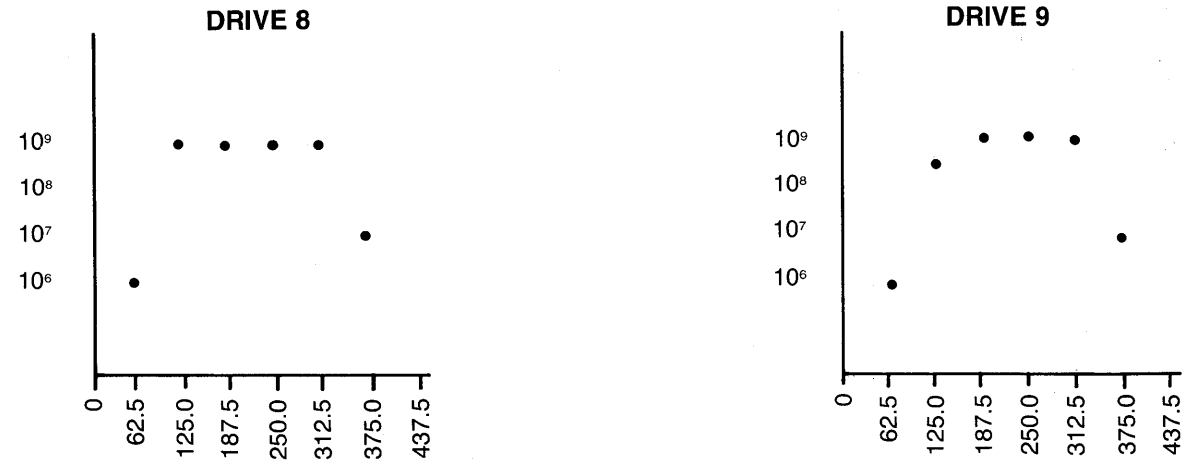
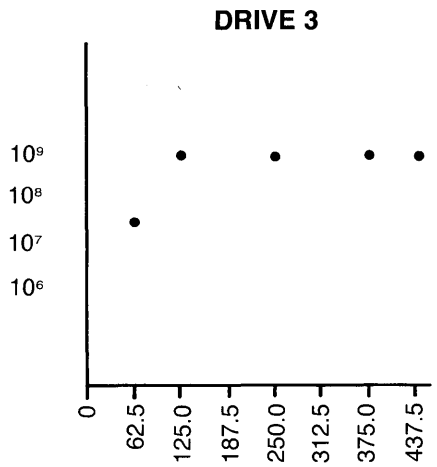
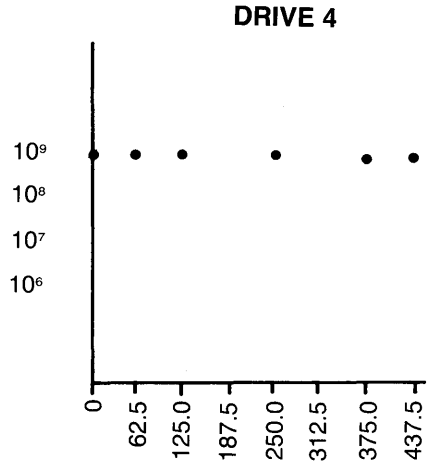
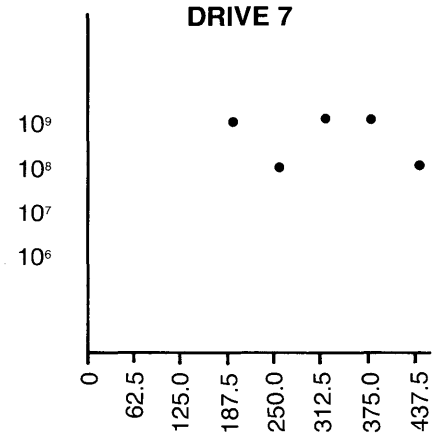
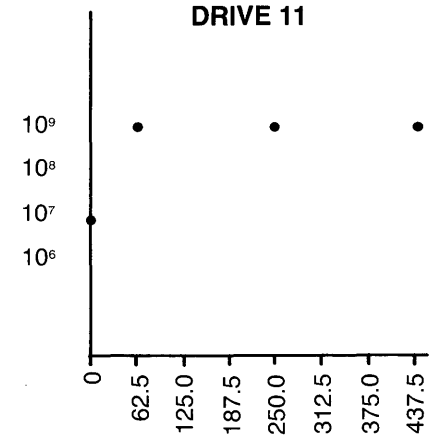


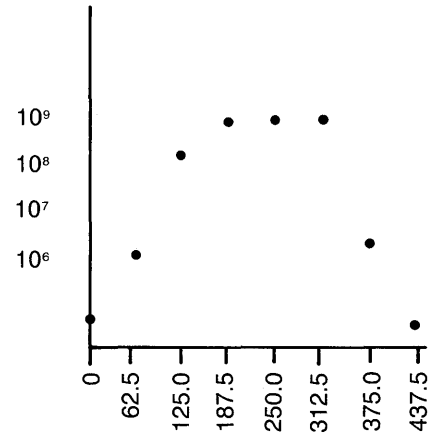
FIGURE 10: 8″ DRIVE WRITE PRECOMPENSATION

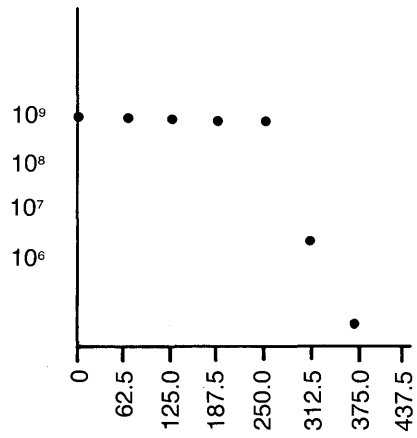

DRIVE 3
10^9
10^8
10^7
10^6
0
62.5
125.0
187.5
250.0
312.5
375.0
437.5


DRIVE 4
10^9
10^8
10^7
10^6
0
62.5
125.0
187.5
250.0
312.5
375.0
437.5


DRIVE 7
10^9
10^8
10^7
10^6
0
62.5
125.0
187.5
250.0
312.5
375.0
437.5


DRIVE 11
10^9
10^8
10^7
10^6
0
62.5
125.0
187.5
250.0
312.5
375.0
437.5


DRIVE 12
10^9
10^8
10^7
10^6
0
62.5
125.0
187.5
250.0
312.5
375.0
437.5


DRIVE 13
10^9
10^8
10^7
10^6
0
62.5
125.0
187.5
250.0
312.5
375.0
437.5

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