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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

# MC146818

*Advance Information*

# REAL-TIME CLOCK PLUS RAM (RTC)

The MC146818 Real-Time Clock plus RAM is a peripheral device which includes the unique MOTEL concept for use with various microprocessors, microcomputers, and larger computers. This part combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The MC146818 uses high-speed CMOS technology to interface with 1 MHz processor buses, while consuming very little power.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS part (in an otherwise NMOS/TTL system) including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the MC146818 may be used with a CMOS microprocessor to relieve the software of the timekeeping workload and to extend the available RAM of an MPU such as the MC146805E2.

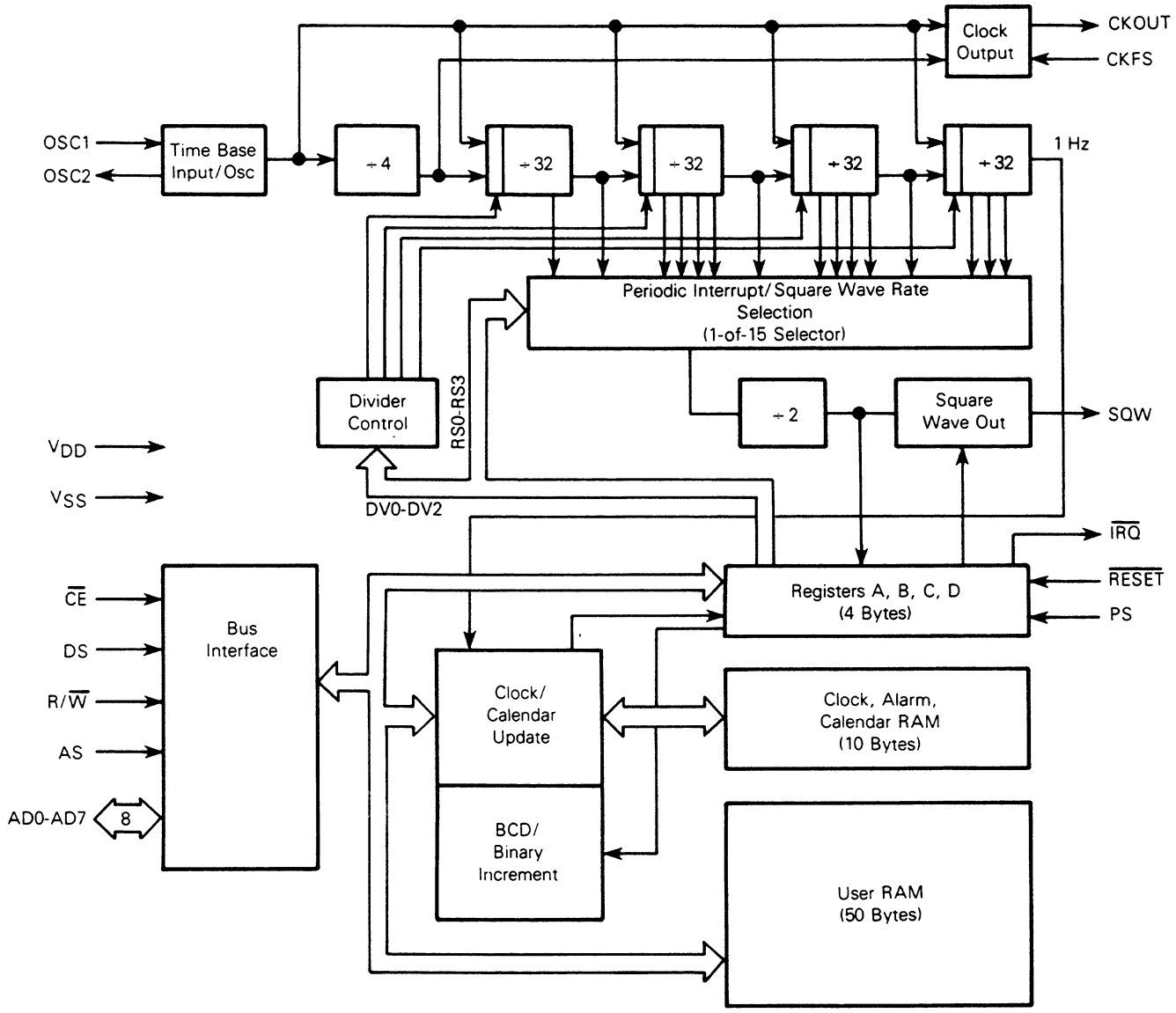
- Low-Power, High-Speed, High-Density CMOS
- Internal Time Base and Oscillator
- Counts Seconds, Minutes, and Hours of the Day
- Counts Days of the Week, Date, Month, and Year
- 3 V to 6 V Operation
- Time Base Input Options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz
- Time Base Oscillator for Parallel Resonant Crystals
- 40 to 200 μW Typical Operating Power at Low Frequency Time Base
- 4.0 to 20 mW Typical Operating Power at High Frequency Time Base
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24-Hour Clock with AM and PM in 12-Hour Mode
- Daylight Savings Time Option
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Microprocessor Bus Compatible
- MOTEL Circuit for Bus Universality
- Multiplexed Bus for Pin Efficiency
- Interfaced with Software as 64 RAM Locations
- 14 Bytes of Clock and Control Registers
- 50 Bytes of General Purpose RAM
- Status Bit Indicates Data Integrity
- Bus Compatible Interrupt Signals ($\overline{IRQ}$)
- Three Interrupts are Separately Software Maskable and Testable
  - Time-of-Day Alarm, Once-per-Second to Once-per-Day
  - Periodic Rates from 30.5 μs to 500 ms
  - End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Clock Output May Be Used as Microprocessor Clock Input
  - At Time Base Frequency ÷ 1 or ÷ 4
- 24-Pin Dual-In-Line Package

This document contains information on a new product. Specifications and information herein are subject to change without notice.



MOTOROLA

FIGURE 1 — BLOCK DIAGRAM




**MAXIMUM RATINGS** (Voltages referenced to $V_{SS}$)

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | −0.3 to +8.0 | V |
| All Input Voltages Except OSC1 | $V_{in}$ | $V_{SS}$−0.5 to $V_{DD}$+0.5 | V |
| Current Drain per Pin Excluding $V_{DD}$ and $V_{SS}$ | I | 10 | mA |
| Operating Temperature Range<br>MC146818<br>MC146818C ($V_{DD}$=3.0 to 5.5 V operation) | $T_A$ | $T_L$ to $T_H$<br>0 to 70<br>−40 to 85 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance<br>Plastic | $\theta_{JA}$ | 120 | °C/W |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$).

**DC ELECTRICAL CHARACTERISTICS** ($V_{DD}$ = 3 Vdc, $V_{SS}$ = 0 Vdc, $T_A = T_L$ to $T_H$ unless otherwise noted)

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Frequency of Operation | $f_{osc}$ | 32.768 | 32.768 | kHz |
| Output Voltage | $V_{OL}$ | – | 0.1 | V |
| $I_{Load} < 10\ \mu A$ | $V_{OH}$ | $V_{DD} - 0.1$ | – | |
| $I_{DD}$ – Bus Idle<br>CKOUT = $f_{osc}$, $C_L$ = 15 pF; SQW Disabled, $\overline{CE} = V_{DD} - 0.2$; $C_L$ (OSC2) = 10 pF<br>$f_{osc}$ = 32.768 kHz | $I_{DD3}$ | – | 50 | μA |
| $I_{DD}$ – Quiescent<br>$f_{osc}$ = DC; OSC1 = DC;<br>All Other Inputs = $V_{DD} - 0.2$ V;<br>No Clock | $I_{DD4}$ | – | 50 | μA |
| Output High Voltage<br>($I_{Load} = -0.25$ mA, All Outputs) | $V_{OH}$ | 2.7 | – | V |
| Output Low Voltage<br>($I_{Load} = 0.25$ mA, All Outputs) | $V_{OL}$ | – | 0.3 | V |
| Input High Voltage — AD0-AD7, DS, AS, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET}$, CKFS, PS, OSC1 | $V_{IH}$ | 2.1<br>2.5 | $V_{DD}$<br>$V_{DD}$ | V |
| Input Low Voltage (All Inputs) | $V_{IL}$ | $V_{SS}$ | 0.5 | V |
| Input Current — All Inputs | $I_{in}$ | – | ±1 | μA |
| Three-State Leakage — $\overline{IRQ}$, AD0-AD7 | $I_{TSL}$ | – | ±10 | μA |

**DC ELECTRICAL CHARACTERISTICS** ($V_{DD}$ = 5 Vdc ±10%, $V_{SS}$ = 0 Vdc, $T_A = T_L$ to $T_H$ unless otherwise noted)

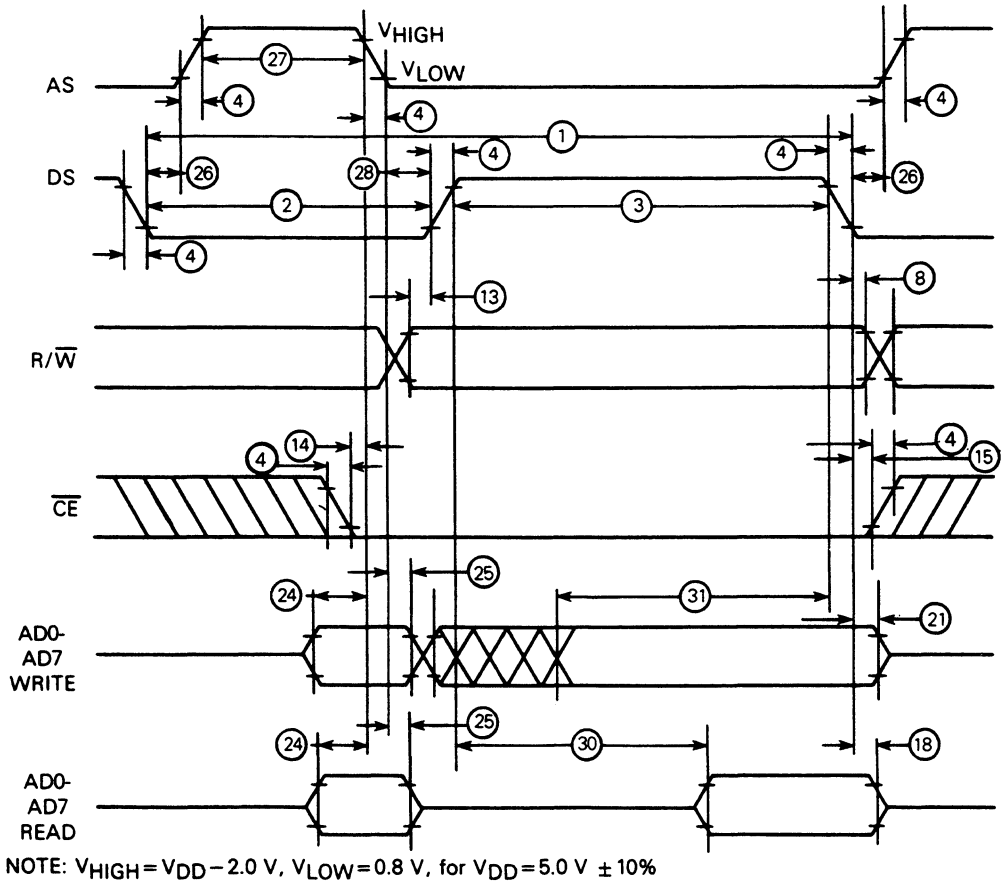
| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Frequency of Operation | $f_{osc}$ | 32.768 | 4194.304 | kHz |
| Output Voltage | $V_{OL}$ | – | 0.1 | V |
| $I_{Load} < 10\ \mu A$ | $V_{OH}$ | $V_{DD} - 0.1$ | – | |
| $I_{DD}$ – Bus Idle (External Clock)<br>CKOUT = $f_{osc}$, $C_L$ = 15 pF; SQW Disabled, $\overline{CE} = V_{DD} - 0.2$; $C_L$ (OSC2) = 10 pF | | | | |
| $f_{osc}$ = 4.194304 MHz | $I_{DD1}$ | – | 3 | mA |
| $f_{osc}$ = 1.048516 MHz | $I_{DD2}$ | – | 800 | μA |
| $f_{osc}$ = 32.768 kHz | $I_{DD3}$ | – | 50 | μA |
| $I_{DD}$ – Quiescent<br>$f_{osc}$ = DC; OSC1 = DC;<br>All Other Inputs = $V_{DD} - 0.2$ V;<br>No Clock | $I_{DD4}$ | – | 50 | μA |
| Output High Voltage<br>($I_{Load} = -1.6$ mA, AD0-AD7, CKOUT)<br>($I_{Load} = -1.0$ mA, SQW) | $V_{OH}$ | 4.1 | – | V |
| Output Low Voltage<br>($I_{Load} = 1.6$ mA, AD0-AD7, CKOUT)<br>($I_{Load} = 1.0$ mA, $\overline{IRQ}$ and SQW) | $V_{OL}$ | – | 0.4 | V |
| Input High Voltage — CKFS, AD0-AD7, DS, AS, R/$\overline{W}$, $\overline{CE}$, PS | $V_{IH}$ | $V_{DD} - 2.0$ | $V_{DD}$ | V |
| $\overline{RESET}$ | | $V_{DD} - 0.8$ | $V_{DD}$ | |
| OSC1 | | $V_{DD} - 1.0$ | $V_{DD}$ | |
| Input Low Voltage — AD0-AD7, DS, AS, R/$\overline{W}$, $\overline{CE}$ | $V_{IL}$ | $V_{SS}$ | 0.8 | V |
| CKFS, PS, $\overline{RESET}$ | | $V_{SS}$ | 0.8 | |
| OSC1 | | $V_{SS}$ | 0.8 | |
| Input Current — All Inputs | $I_{in}$ | – | ±1 | μA |
| Three-State Leakage — $\overline{IRQ}$, AD0-AD7 | $I_{TSL}$ | – | ±10 | μA |

## BUS TIMING

| Ident. Number | Characteristics | Symbol | $V_{DD}$ = 3.0 V 50 pF Load | | $V_{DD}$ = 5.0 V ± 10% 2 TTL and 130 pF Load | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | Cycle Time | $t_{cyc}$ | 5000 | – | 953 | dc | ns |
| 2 | Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High | $PW_{EL}$ | 1000 | – | 300 | – | ns |
| 3 | Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low | $PW_{EH}$ | 1500 | – | 325 | – | ns |
| 4 | Input Rise and Fall Time | $t_r$, $t_f$ | – | 100 | – | 30 | ns |
| 8 | R/$\overline{W}$ Hold Time | $t_{RWH}$ | 10 | – | 10 | – | ns |
| 13 | R/$\overline{W}$ Setup Time Before DS/E | $t_{RWS}$ | 200 | – | 80 | – | ns |
| 14 | Chip Enable Setup Time Before AS/ALE Fall | $t_{CS}$ | 200 | * | 55 | * | ns |
| 15 | Chip Enable Hold Time | $t_{CH}$ | 10 | – | 0 | – | ns |
| 18 | Read Data Hold Time | $t_{DHR}$ | 10 | 1000 | 10 | 100 | ns |
| 21 | Write Data Hold Time | $t_{DHW}$ | 100 | – | 0 | – | ns |
| 24 | Muxed Address Valid Time to AS/ALE Fall | $t_{ASL}$ | 200 | – | 50 | – | ns |
| 25 | Muxed Address Hold Time | $t_{AHL}$ | 100 | – | 20 | – | ns |
| 26 | Delay Time DS/E to AS/ALE Rise | $t_{ASD}$ | 500 | – | 50 | – | ns |
| 27 | Pulse Width, AS/ALE High | $PW_{ASH}$ | 600 | – | 135 | – | ns |
| 28 | Delay Time, AS/ALE to DS/E Rise | $t_{ASED}$ | 500 | – | 60 | – | ns |
| 30 | Peripheral Output Data Delay Time from DS/E or $\overline{RD}$ | $t_{DDR}$ | 1300 | – | 20 | 240 | ns |
| 31 | Peripheral Data Setup Time | $t_{DSW}$ | 1500 | – | 200 | – | ns |

NOTE: Designations E, ALE, $\overline{RD}$, and $\overline{WR}$ refer to signals from alternative microprocessor signals.
*Refer to **IMPORTANT NOTICES** appearing on page 20 of this data sheet.

**FIGURE 2 — MC146818 BUS TIMING**




NOTE: $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 10%

FIGURE 3 — BUS READ TIMING COMPETITOR MULTIPLEXED BUS

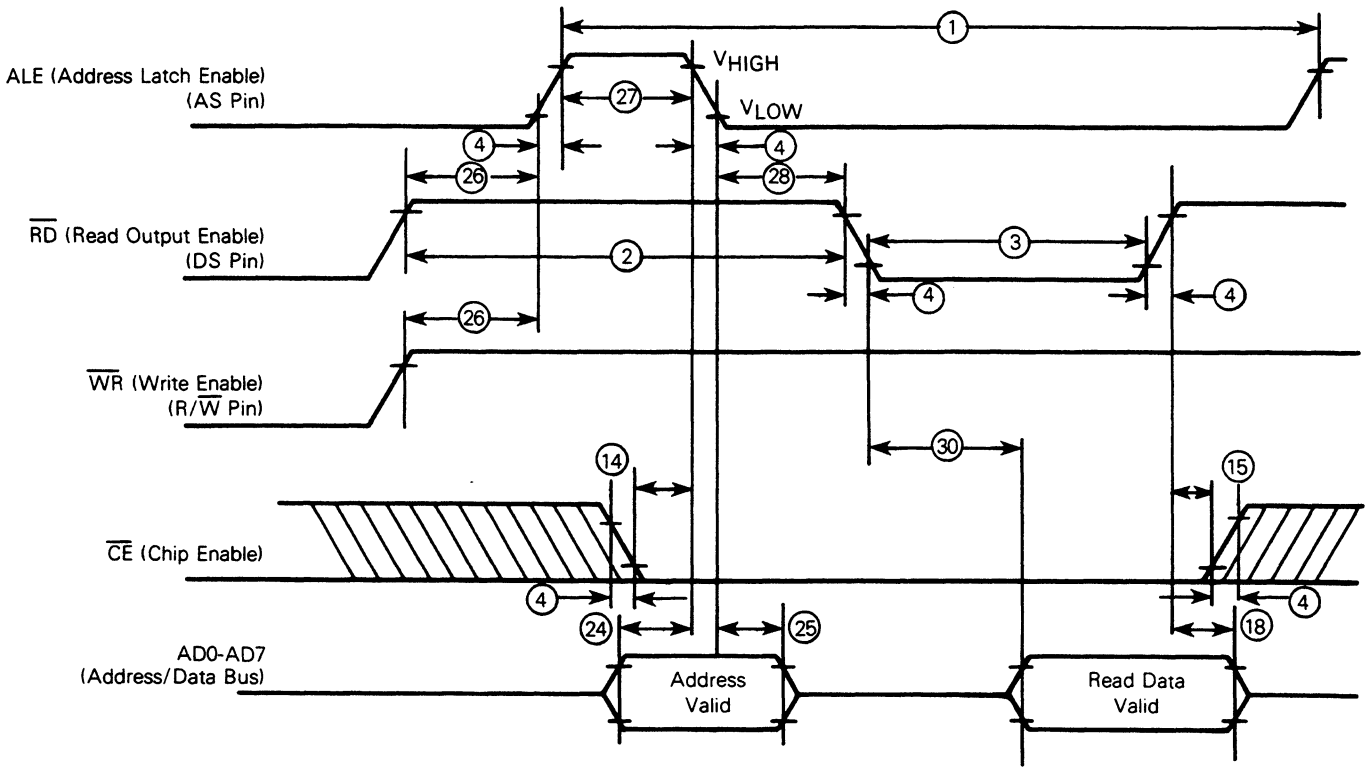
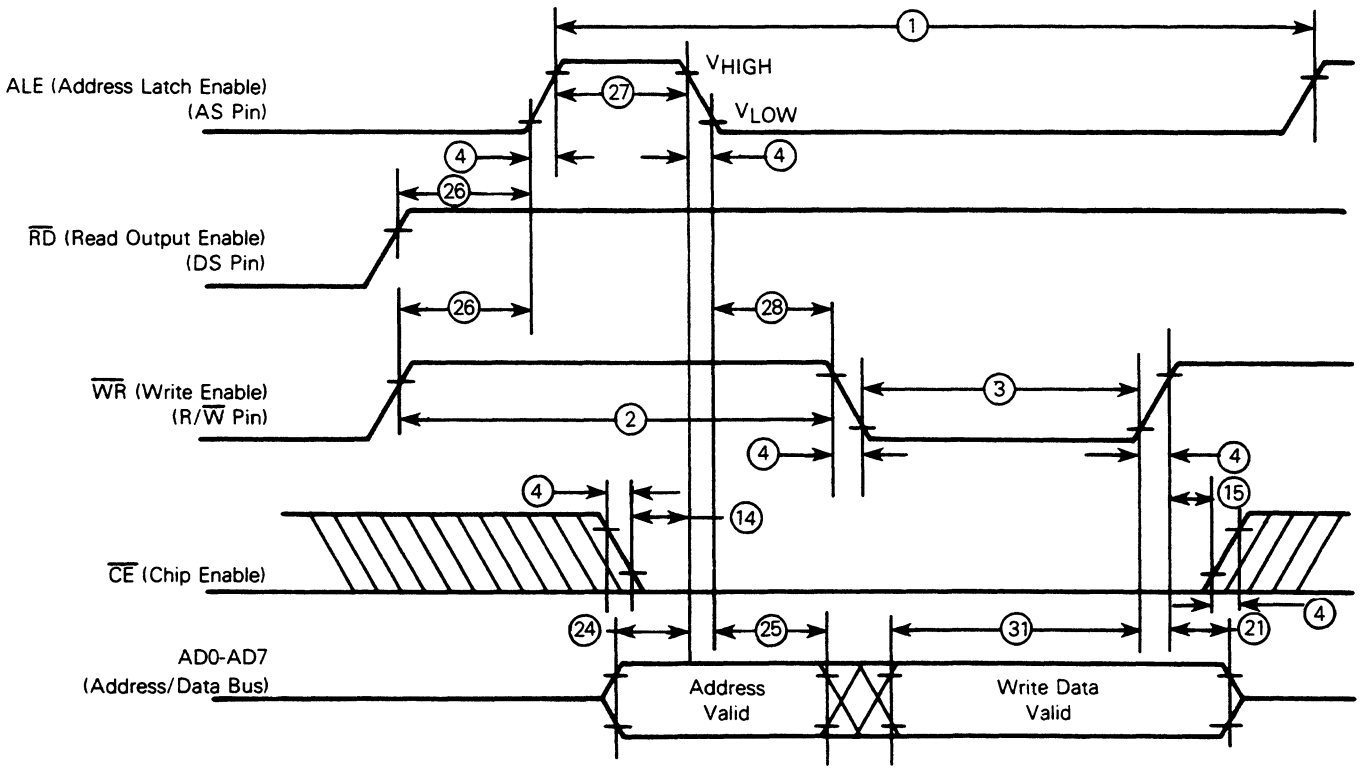



FIGURE 4 — BUS WRITE TIMING COMPETITOR MULTIPLEXED BUS

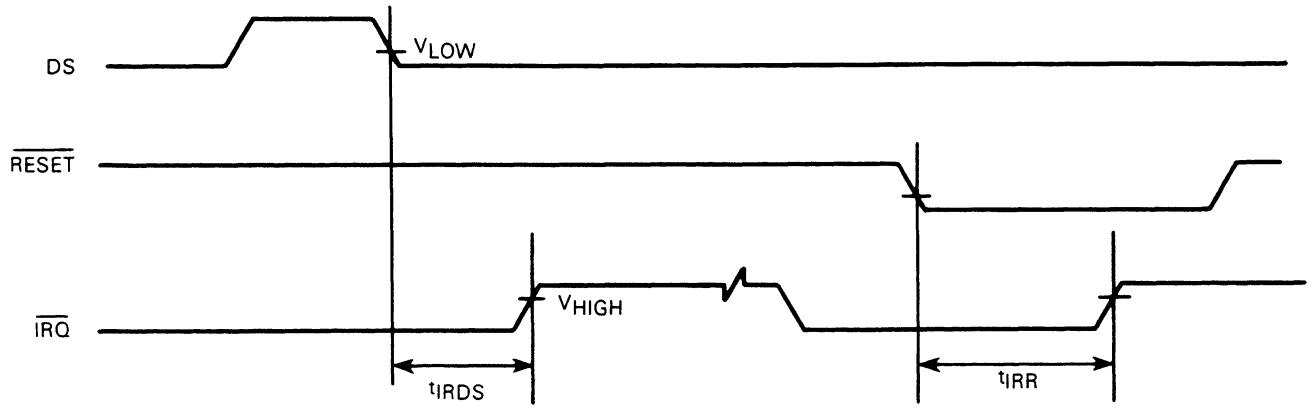



NOTE: $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 10%

**TABLE 1 — SWITCHING CHARACTERISTICS** ($V_{DD}$ = 5.0 Vdc ± 10%, $V_{SS}$ = 0 Vdc, $T_A = T_L$ to $T_H$)

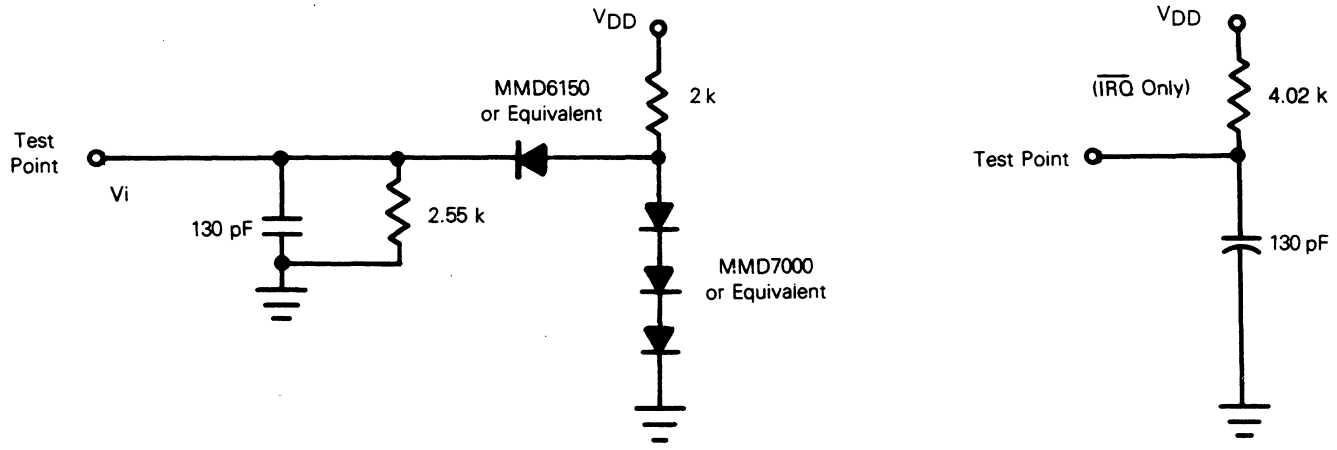
| Description | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Oscillator Startup | $t_{RC}$ | — | 100 | ms |
| Reset Pulse Width | $t_{RWL}$ | 5 | — | μs |
| Reset Delay Time | $t_{RLH}$ | 5 | — | μs |
| Power Sense Pulse Width | $t_{PWL}$ | 5 | — | μs |
| Power Sense Delay Time | $t_{PLH}$ | 5 | — | μs |
| $\overline{IRQ}$ Release from DS | $t_{IRDS}$ | — | 2 | μs |
| $\overline{IRQ}$ Release from $\overline{RESET}$ | $t_{IRR}$ | — | 2 | μs |
| VRT Bit Delay | $t_{VRTD}$ | — | 2 | μs |

**FIGURE 5 — $\overline{IRQ}$ RELEASE DELAY**




NOTE: $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 10%

**FIGURE 6 — TTL EQUIVALENT TEST LOAD**




All Outputs Except OSC2 (See Figure 10)

FIGURE 7 — POWER-UP

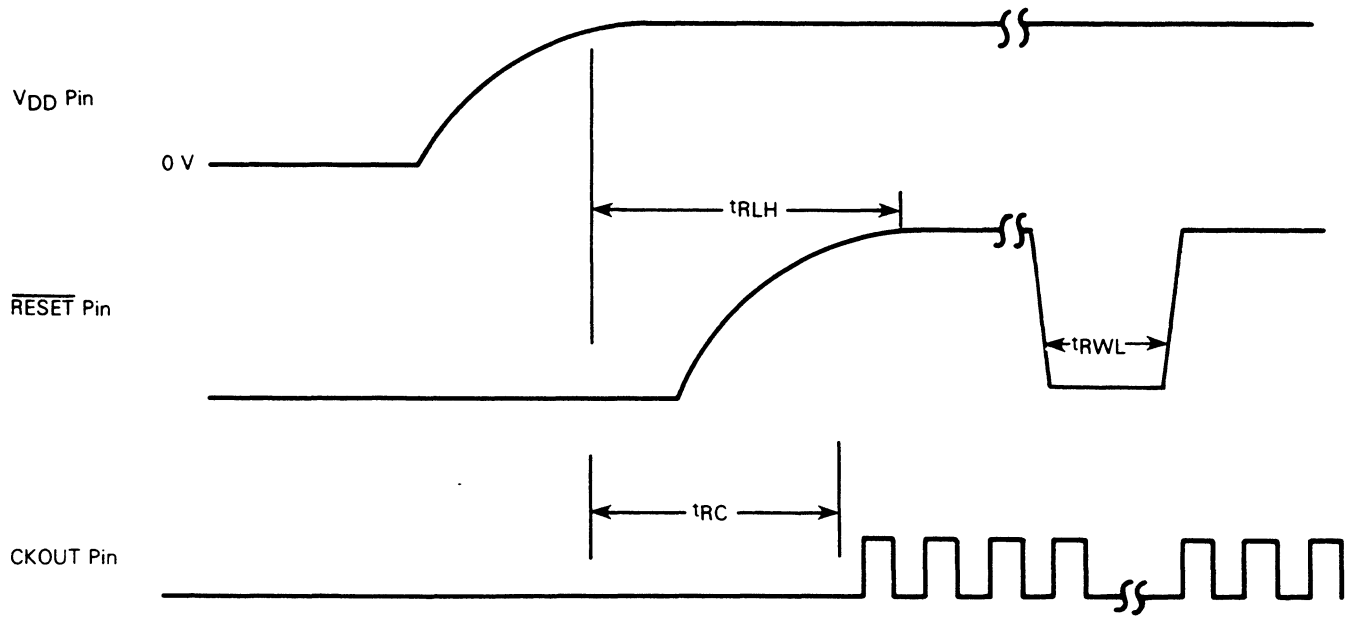
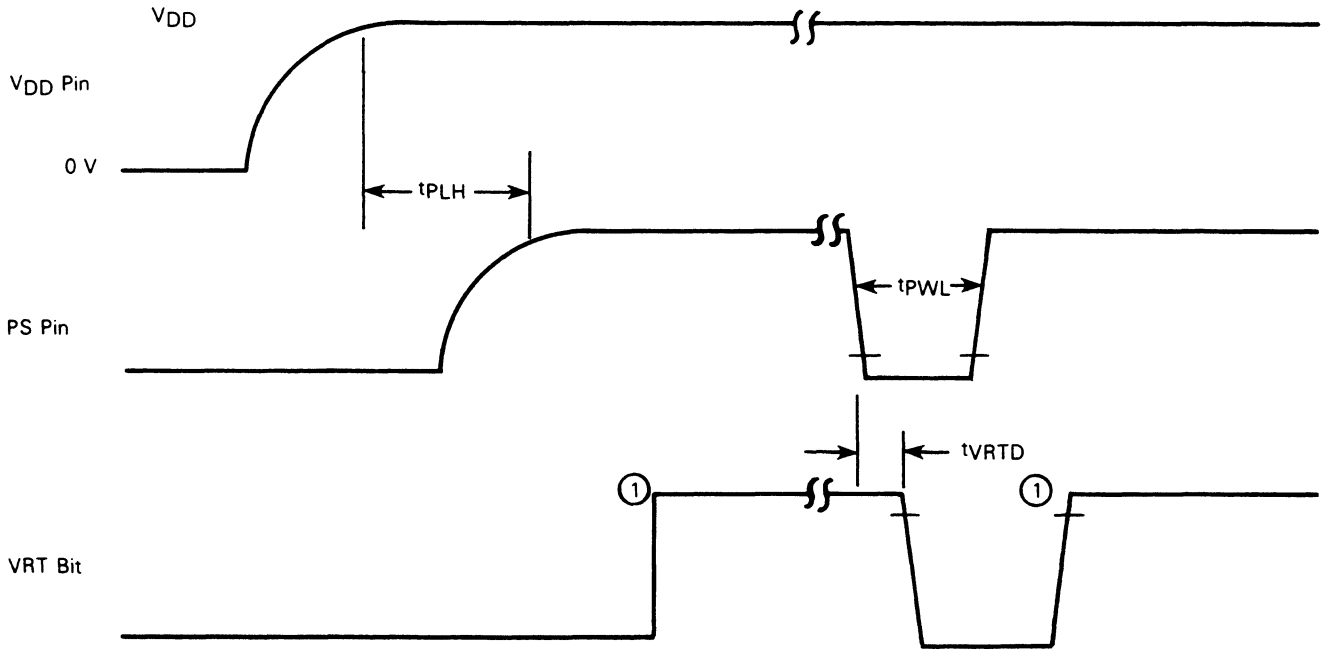



FIGURE 8 — CONDITIONS THAT CLEAR VRT BIT




(1) The VRT bit is set to a "1" by reading Register d. The VRT bit can only be cleared by pulling the PS pin low (see **REGISTER D ($0D)**).

## MOTEL

The MOTEL circuit is a new concept that permits the MC146818 to be directly interfaced with many types of microprocessors. No external logic is needed to adapt to the differences in bus control signals from common multiplexed bus microprocessors.

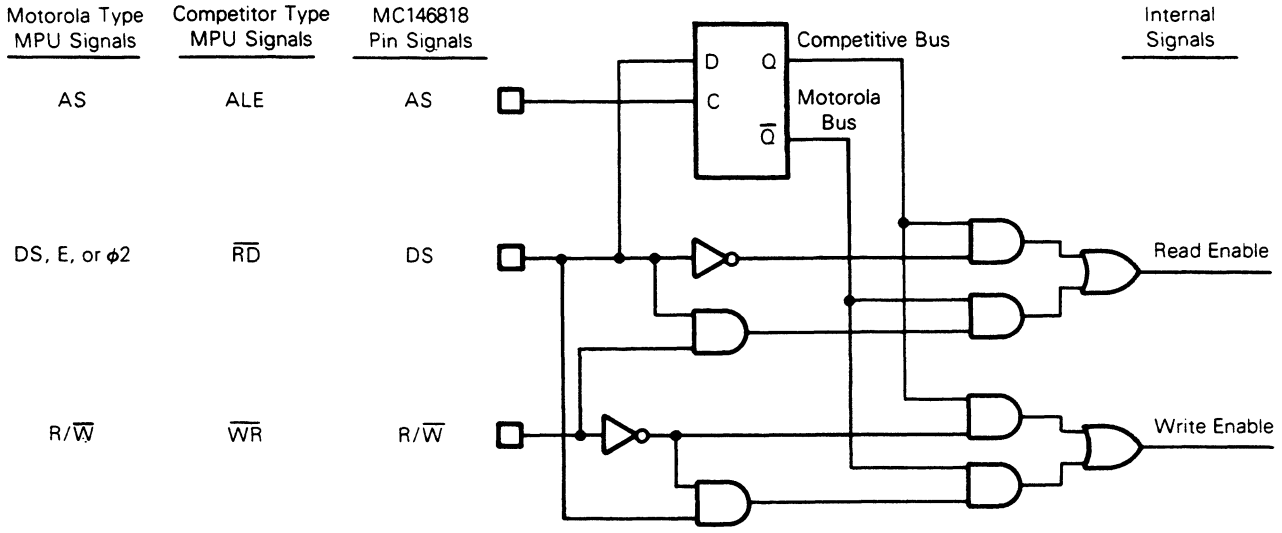
Practically all microprocessors interface with one of two synchronous bus structures. One bus was originated by the Motorola MC6800 and the other by the Intel 8080 and its companion part, the 8228.

The MOTEL circuit (for MOTorola and IntEL bus compatibility) is built into peripheral and memory ICs to permit direct connection to either type of bus. An industry standard bus structure is now available. The MOTEL concept is shown logically in Figure 9.

MOTEL selects one of two interpretations of two pins. In the Motorola case, DS and R/$\overline{W}$ are gated together to produce the internal read enable. The internal write enable is a similar gating of the inverse of R/$\overline{W}$. With competitor buses, the inversion of $\overline{RD}$ and $\overline{WR}$ create functionally identical internal read and write enable signals.

The MC146818 automatically selects the processor type by using AS/ALE to latch the state of the DS/$\overline{RD}$ pin. Since DS is always low and $\overline{RD}$ is always high during AS and ALE, the latch automatically indicates which processor type is connected.

FIGURE 9 — FUNCTIONAL DIAGRAM OF MOTEL CIRCUIT




## SIGNAL DESCRIPTIONS

The block diagram in Figure 1, shows the pin connection with the major internal functions of the MC146818 Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

### $V_{DD}$, $V_{SS}$

DC power is provided to the part on these two pins, $V_{DD}$ being the more positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

### OSC1, OSC2 — TIME BASE, INPUTS

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC1 as shown in Figure 10. The internal time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant AT cut crystal at 4.194304 MHz or 1.048576 MHz frequencies. The crystal connections are shown in Figure 11 and the crystal characteristics in Figure 12.

### CKOUT — CLOCK OUT, OUTPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 2.

### CKFS — CLOCK OUT FREQUENCY SELECT, INPUT

When the CKFS pin is tied to $V_{DD}$ it causes CKOUT to be the same frequency as the time base at the OSC1 pin. When CKFS is tied to $V_{SS}$, CKOUT is the OSC1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS.

FIGURE 10 — EXTERNAL TIME-BASE CONNECTION

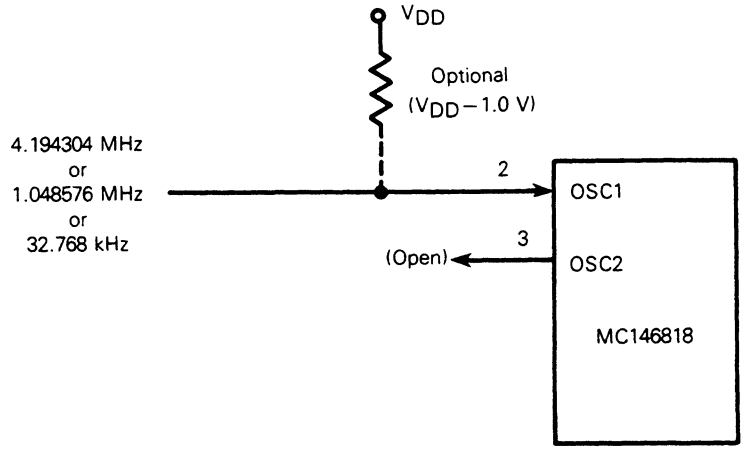
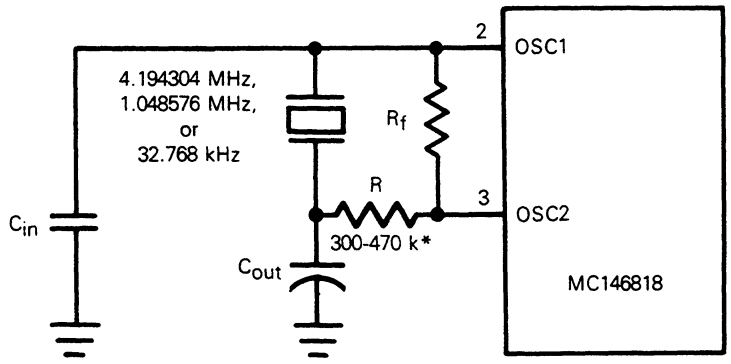


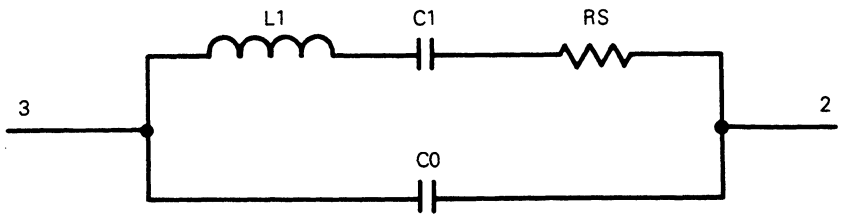

FIGURE 11 — CRYSTAL OSCILLATOR CONNECTION

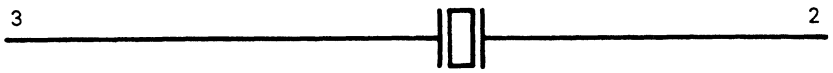



*32.768 kHz Only — Consult Crystal Manufacturer's Specification

FIGURE 12 — CRYSTAL PARAMETERS

Crystal Equivalent Circuit




| $f_{osc}$ | 4.194304 MHz | 1.048576 MHz | 32.768 kHz |
|---|---|---|---|
| RS (Maximum) | 75 Ω | 700 Ω | 50 k |
| C0 (Maximum) | 7 pF | 5 pF | 1.7 pF |
| C1 | 0.012 pF | 0.008 pF | 0.003 pF |
| Q | 50 k | 35 k | 30 k |
| $C_{in}/C_{out}$ | 15-30 pF | 15-40 pF | 10-22 pF |
| R | — | — | 300-470 k |
| $R_f$ | 10 M | 10 M | 22 M |

ıain high during the time AS/ALE is

**E, INPUT**

reats the R/$\overline{W}$ pin in one of two ways.
ıe processor is connected, R/$\overline{W}$ is a
vhether the current cycle is a read or
indicated with a high level on R/$\overline{W}$
eas a write cycle is a low on R/$\overline{W}$ dur-

tation of R/$\overline{W}$ is as a negative write
and $\overline{I/OW}$ from competitor type pro-
ircuit in this mode gives R/$\overline{W}$ pin the
write (W) pulse on many generic

**INPUT**

$\overline{E}$) signal must be asserted (low) for a
MC146818 is to be accessed. $\overline{CE}$ is not
stable during DS and AS (Motorola
during $\overline{RD}$ and $\overline{WR}$ (in the other
cles which take place without asserting
to take place within the MC146818.
multiplexed bus output is in a high-

ll address, data, DS, and R/$\overline{W}$ inputs
e disconnected within the MC146818.
46818 to be isolated from a powered-
ıen $\overline{CE}$ is held high, an unpowered
power through the input pins from the
source. Battery power consumption
by using a pullup resistor or active
main power is off. When $\overline{CE}$ is not us-
ıded.

**EQUEST, OUTPUT**

tive low output of the MC146818 that
errupt input to a processor. The $\overline{IRQ}$
long as the status bit causing the in-
the corresponding interrupt-enable bit
pin, the processor program normally
$\overline{RESET}$ pin also clears pending inter-

onditions are present, the $\overline{IRQ}$ level is
e state. Multiple interrupting devices
d to an $\overline{IRQ}$ bus with one pullup at the

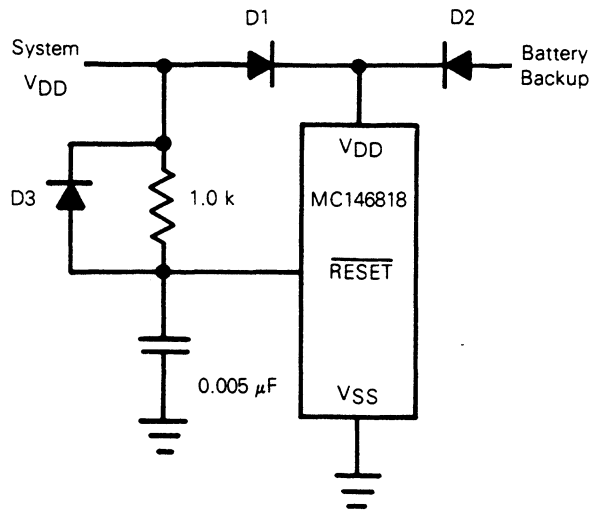
**PUT**

ıes not affect the clock, calendar, or
ıowerup, the $\overline{RESET}$ pin must be held
ime, $t_{RLH}$, in order to allow the power
gure 13 shows a typical representation
uit.
the following occurs:
ot Enable (PIE) bit is cleared to zero,
Enable (AIE) bit is cleared to zero,
nterrupt Enable (UIE) bit is cleared to

ıterrupt Flag (UF) bit is cleared to zero,
st status Flag (IRQF) bit is cleared to

ot Flag (PF) bit is cleared to zero,
accessible.

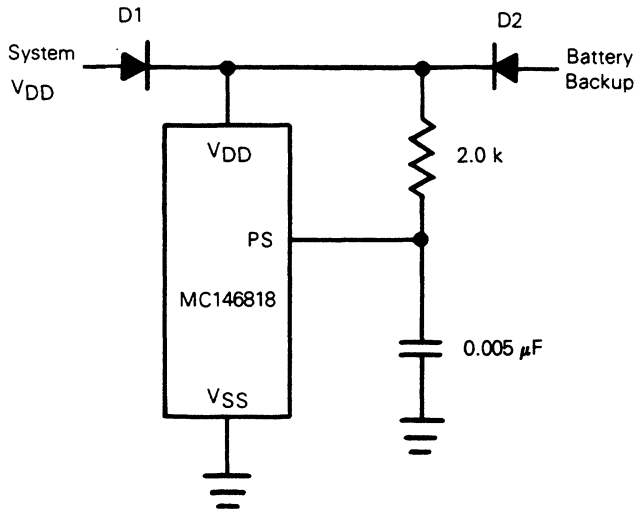
FIGURE 13 — TYPICAL POWERUP DELAY CIRCUIT FOR $\overline{\text{RESET}}$




D1 = MBD701 (Schottky) or Equivalent
D2 = D3 = 1N4148 or Equivalent

Note: If the RTC is isolated from the MPU or MCU power by a diode drop, care must be taken to meet $V_{in}$ requirements.

FIGURE 14 — TYPICAL POWERUP DELAY CIRCUIT FOR POWER SENSE




D1 = MBD701 (Schottky) or Equivalent
D2 = 1N4148 or Equivalent

g) Alarm Interrupt Flag (AF) bit is cleared to zero,
h) $\overline{\text{IRQ}}$ pin is in high-impedance state, and
i) Square Wave output Enable (SQWE) bit is cleared to zero.

### PS — POWER SENSE, INPUT

The power-sense pin is used in the control of the valid RAM and time (VRT) bit in Register D. When the PS pin is low the VRT bit is cleared to zero.

When using the VRT feature during powerup, the PS pin must be externally held low for the specified $t_{PLH}$ time. As power is applied, the VRT bit remains low indicating that the contents of the RAM, time registers, and calendar are not guaranteed. PS must go high after powerup to allow the VRT bit to be set by a read of register D.

## POWER-DOWN CONSIDERATIONS

In most systems, the MC146818 must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made. During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimize power consumption, and ensure hardware reliability.

The chip enable ($\overline{\text{CE}}$) pin controls all bus inputs (R/$\overline{\text{W}}$, DS, AS, AD0-AD7). $\overline{\text{CE}}$, when negated, disallows any unintended modification of the RTC data by the bus. $\overline{\text{CE}}$ also reduces power consumption by reducing the number of transitions seen internally.

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the squarewave (SQW) pin.

During and after the power source conversion, the $V_{IN}$ maximum specification must never be exceeded. Failure to meet the $V_{IN}$ maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part.

## ADDRESS MAP

Figure 15 shows the address map of the MC146818. The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writable by the processor program except for the following: 1) Registers C and D are read only, 2) bit 7 of Register A is read only, and 3) the high-order bit of the seconds byte is read only. The contents of four control and status registers (A, B, C, and D) are described in **REGISTERS.**

### TIME, CALENDAR, AND ALARM LOCATIONS

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

Table 3 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1".

The time, calendar, and alarm bytes are not always accessable by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248 $\mu$s at the 4.194304 MHz and 1.048567 MHz time bases and 1948 $\mu$s for the 32.768 kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

FIGURE 15 — ADDRESS MAP

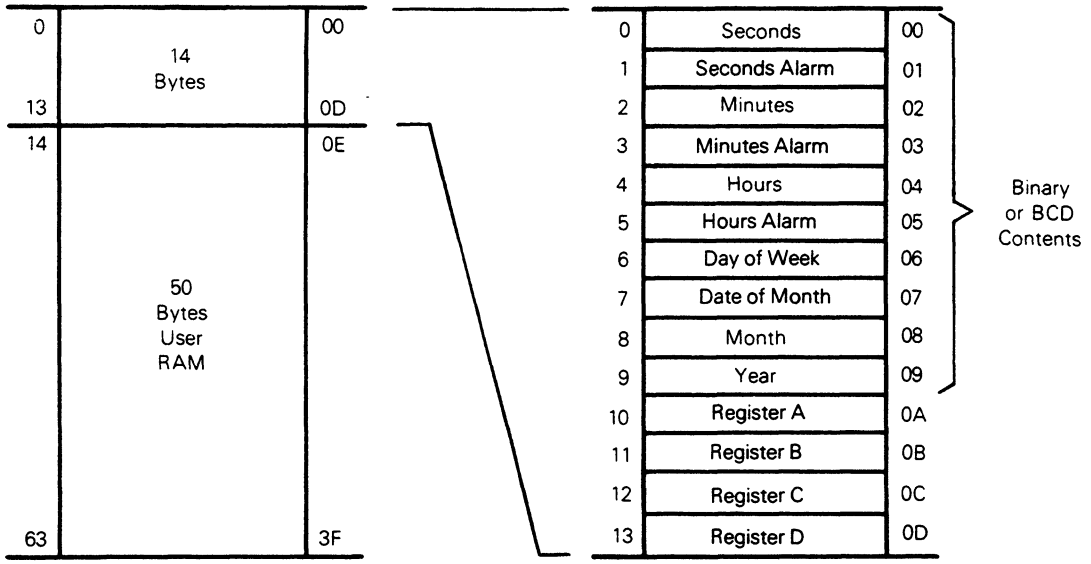



TABLE 3 — TIME, CALENDAR, AND ALARM DATA MODES

| Address Location | Function | Decimal Range | Range | | Example* | |
|---|---|---|---|---|---|---|
| | | | Binary Data Mode | BCD Data Mode | Binary Data Mode | BCD Data Mode |
| 0 | Seconds | 0-59 | $00-$3B | $00-$59 | 15 | 21 |
| 1 | Seconds Alarm | 0-59 | $00-$3B | $00-$59 | 15 | 21 |
| 2 | Minutes | 0-59 | $00-$3B | $00-$59 | 3A | 58 |
| 3 | Minutes Alarm | 0-59 | $00-$3B | $00-$59 | 3A | 58 |
| 4 | Hours (12 Hour Mode) | 1-12 | $01-$0C (AM) and $81-$8C (PM) | $01-$12 (AM) and $81-$92 (PM) | 05 | 05 |
| | Hours (24 Hour Mode) | 0-23 | $00-$17 | $00-$23 | 05 | 05 |
| 5 | Hours Alarm (12 Hour Mode) | 1-12 | $01-$0C (AM) and $81-$8C (PM) | $01-$12 (AM) and $81-$92 (PM) | 05 | 05 |
| | Hours Alarm (24 Hour Mode) | 0-23 | $00-$17 | $00-23 | 05 | 05 |
| 6 | Day of the Week Sunday = 1 | 1-7 | $01-$07 | $01-$07 | 05 | 05 |
| 7 | Date of the Month | 1-31 | $01-$1F | $01-$31 | 0F | 15 |
| 8 | Month | 1-12 | $01-$0C | $01-$12 | 02 | 02 |
| 9 | Year | 0-99 | $00-$63 | $00-$99 | 4F | 79 |

*Example: 5:58:21 Thursday 15 February 1979 (time is AM)

rrupt event occurs a flag bit is set to a "1" in
n of the three interrupt sources have separate
ter C, which are set independent of the state
nding enable bits in Register B. The flag bit
ith or without enabling the corresponding

are scanned case, the program does not
rupt. The "interrupt" flag bit becomes a
the software interrogates, when it wishes.
are detects that the flag is set, it is an indica-
that the "interrupt" event occurred since the
l.

e is one precaution. The flag bits in Register
ecord of the interrupt event is erased) when
d. Double latching is included with Register
hich are set are stable throughout the read
hich are high when read by the program are
v interrupts (on any bits) are held until after
)ne, two, or three flag bits may be found to
gister C is read. The program should inspect
bits every time Register C is read to insure
ts are lost.
lag bit usage method is with fully enabled
n an interrupt-flag bit is set and the cor-
rrupt-enable bit is also set, the $\overline{IRQ}$ pin is
$\overline{Q}$ is asserted as long as at least one of the
ources has its flag and enable bits both set.
Register C is a "1" whenever the $\overline{IRQ}$ pin is
/.
r program can determine that the RTC
rrupt by reading Register C. A "1" in bit 7
ates that one or more interrupts have been
part. The act of reading Register C clears all
flag bits, plus the IRQF bit. When the pro-
set, it should look at each of the individual
same byte which have the corresponding
bits set and service each interrupt which is
e than one interrupt-flag bit may be set.

## DIVIDER STAGES

3 has 22 binary-divider stages following the
wn in Figure 1. The output of the dividers is
he update-cycle logic. The dividers are con-
livider bus (DV2, DV1, and DV0) in Register

## ROL

ntrol bits have three uses, as shown in Table
e operating time bases may be selected
1.048576 MHz, or 32.768 kHz). The divider
eld reset, which allows precision setting of
the divider is changed from reset to an
ase, the first update cycle is one-half second
er-control bits are also used to facilitate
46818.

TABLE 4 — DIVIDER CONFIGURATIONS

| Time-Base Frequency | Divider Bits Register A | | | Operation Mode | Divider Reset | Bypass First N-Divider Bits |
|---|---|---|---|---|---|---|
| | DV2 | DV1 | DV0 | | | |
| 4.194304 MHz | 0 | 0 | 0 | Yes | – | N = 0 |
| 1.048576 MHz | 0 | 0 | 1 | Yes | – | N = 2 |
| 32.768 kHz | 0 | 1 | 0 | Yes | – | N = 7 |
| Any | 1 | 1 | 0 | No | Yes | – |
| Any | 1 | 1 | 1 | No | Yes | – |

Note: Other combinations of divider bits are used for test purposes only.

## SQUARE-WAVE OUTPUT SELECTION

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 1. The first purpose of selecting a divider tap is to generate a square-wave output signal at the SQW pin. The RS0-RS3 bits in Register A establish the square-wave frequency as listed in Table 5. The SQW frequency selection shares the 1-of-15 selector with periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave enable (SQWE) bit in Register B. Altering the divider, square-wave output selection bits, or the SQWE output-enable bit may generate an asymmetrical waveform at the time of execution. The square-wave output pin has a number of potential uses. For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control.

## PERIODIC INTERRUPT SELECTION

The periodic interrupt allows the $\overline{IRQ}$ pin to be triggered from once every 500 ms to once every 30.517 μs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Table 5 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit in Register B. Similarly the periodic interrupt is enabled by the PIE bit in Register B.

Periodic interrupt is usable by practically all real-time systems. It can be used to scan for all forms of inputs from contact closures to serial receive bits or bytes. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.

TABLE 5 — PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

| Select Bits Register A | | | | 4.194304 or 1.048576 MHz Time Base | | 32.768 kHz Time Base | |
|---|---|---|---|---|---|---|---|
| RS3 | RS2 | RS1 | RS0 | Periodic Interrupt Rate $t_{PI}$ | SQW Output Frequency | Periodic Interrupt Rate $t_{PI}$ | SQW Output Frequency |
| 0 | 0 | 0 | 0 | None | None | None | None |
| 0 | 0 | 0 | 1 | 30.517 μs | 32.768 kHz | 3.90625 ms | 256 Hz |
| 0 | 0 | 1 | 0 | 61.035 μs | 16.384 kHz | 7.8125 ms | 128 Hz |
| 0 | 0 | 1 | 1 | 122.070 μs | 8.192 kHz | 122.070 μs | 8.192 kHz |
| 0 | 1 | 0 | 0 | 244.141 μs | 4.096 kHz | 244.141 μs | 4.096 kHz |
| 0 | 1 | 0 | 1 | 488.281 μs | 2.048 kHz | 488.281 μs | 2.048 kHz |
| 0 | 1 | 1 | 0 | 976.562 μs | 1.024 kHz | 976.562 μs | 1.024 kHz |
| 0 | 1 | 1 | 1 | 1.953125 ms | 512 Hz | 1.953125 ms | 512 Hz |
| 1 | 0 | 0 | 0 | 3.90625 ms | 256 Hz | 3.90625 ms | 256 Hz |
| 1 | 0 | 0 | 1 | 7.8125 ms | 128 Hz | 7.8125 ms | 128 Hz |
| 1 | 0 | 1 | 0 | 15.625 ms | 64 Hz | 15.625 ms | 64 Hz |
| 1 | 0 | 1 | 1 | 31.25 ms | 32 Hz | 31.25 ms | 32 Hz |
| 1 | 1 | 0 | 0 | 62.5 ms | 16 Hz | 62.5 ms | 16 Hz |
| 1 | 1 | 0 | 1 | 125 ms | 8 Hz | 125 ms | 8 Hz |
| 1 | 1 | 1 | 0 | 250 ms | 4 Hz | 250 ms | 4 Hz |
| 1 | 1 | 1 | 1 | 500 ms | 2 Hz | 500 ms | 2 Hz |

## UPDATE CYCLE

The MC146818 executes an update cycle once-per-second, assuming one of the proper time bases is in place, the DV0-DV2 divider is not clear, and the SET bit in Register B is clear. The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 4.194304 MHz or 1.048576 MHz time base the update cycle takes 248 $\mu$s while a 32.768 kHz time base update cycle takes 1984 $\mu$s. During the update cycle, the time, calendar, and alarm bytes are not accessable by the processor program. The MC146818 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update in progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating nonavailability during update are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. During this time a display could be updated or the information could be transfered to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 $\mu$s later. Therefore, if a low is read on the UIP bit, the user has at least 244 $\mu$s before the time/calendar data will be changed. If a "1" is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 $\mu$s.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 16). Periodic interrupts that occur at a rate of greater than $t_{BUC} + t_{UC}$ allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within $(T_{PI} \div 2) + t_{BUC}$ to ensure that data is not read during the update cycle.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the rollover will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

## REGISTERS

The MC146818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

### REGISTER A ($0A)

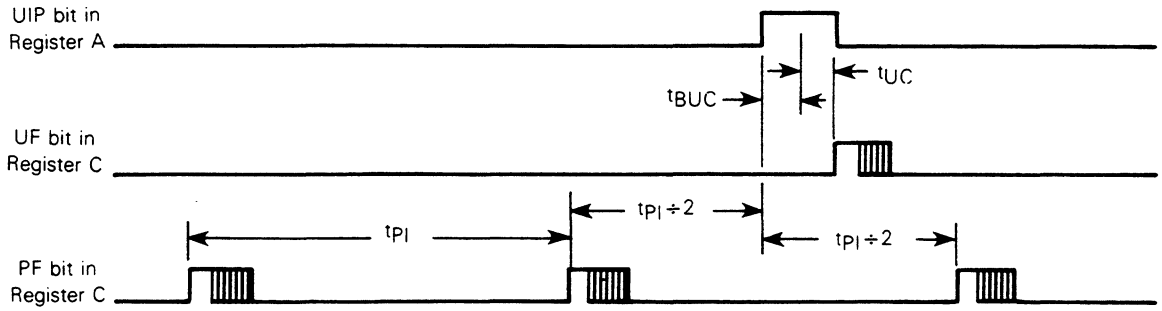
| MSB | | | | | | | LSB | Read/Write |
|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Register |
| UIP | DV2 | DV1 | DV0 | RS3 | RS2 | RS1 | RS0 | except UIP |

**UIP** – The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 $\mu$s (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero – it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibit any update cycle and then clear the UIP status bit.

**TABLE 6 – UPDATE CYCLE TIMES**

| UIP Bit | Time Base (OSC1) | Update Cycle Time ($t_{UC}$) | Minimum Time Before Update Cycle ($t_{BUC}$) |
|---|---|---|---|
| 1 | 4.194304 MHz | 248 $\mu$s | – |
| 1 | 1.048576 MHz | 248 $\mu$s | – |
| 1 | 32.768 kHz | 1984 $\mu$s | – |
| 0 | 4.194304 MHz | – | 244 $\mu$s |
| 0 | 1.048576 MHz | – | 244 $\mu$s |
| 0 | 32.768 kHz | – | 244 $\mu$s |

FIGURE 16 – UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIPS




$t_{PI}$ = Periodic Interrupt Time Interval (500 ms, 250 ms, 125 ms, 62.5 ms, etc. per Table 5)
$t_{UC}$ = Update Cycle Time (248 $\mu$s or 1984 $\mu$s)
$t_{BUC}$ = Delay Time Before Update Cycle (244 $\mu$s)

Three bits are used to permit the pro-
us conditions of the 22-stage divider
lection bits identify which of the three
s is in use. Table 4 shows that time
Hz, 1.048576 MHz, and 32.768 kHz may
selection bits are also used to reset the
the time/calendar is first initialized, the
ne divider at the precise time stored in
divider reset is removed the first update
f second later. These three read/write
by $\overline{\text{RESET}}$.

**S0** – The four rate selection bits select
22-stage divider, or disable the divider
ted may be used to generate an output
in) and/or a periodic interrupt. The pro-
the following: 1) enable the interrupt
enable the SQW output pin with the
both at the same time at the same rate,
Table 5 lists the periodic interrupt rates
frequencies that may be chosen with
ur bits are read/write bits which are not

LSB

| b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| IE | SQWE | DM | 24/12 | DSE |

Read/Write Register

SET bit is a "0", the update cycle func-
dvancing the counts once-per-second.
written to a "1", any update cycle in
nd the program may initialize the time
ithout an update occurring in the midst
a read/write bit which is not modified
functions of the MC146818.

odic interrupt enable (PIE) bit is a
allows the periodic-interrupt flag (PF)
use the $\overline{\text{IRQ}}$ pin to be driven low. A pro-
the PIE bit in order to receive periodic
specified by the RS3, RS2, RS1, and
A. A zero in PIE blocks $\overline{\text{IRQ}}$ from being
interrupt, but the periodic flag (PF) bit
odic rate. PIE is not modified by any in-
unctions, but is cleared to "0" by a

nterrupt enable (AIE) bit is a read/write
a "1" permits the alarm flag (AF) bit in
$\overline{\text{RQ}}$. An alarm interrupt occurs for each
time bytes equal the three alarm bytes
are" alarm code of binary 11XXXXXX).
"0", the AF bit does not initiate an $\overline{\text{IRQ}}$
in clears AIE to "0". The internal func-
ne AIE bit.

pdate-ended interrupt enable) bit is a
enables the update-end flag (UF) bit in
$\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the
lears the UIE bit.

e square-wave enable (SQWE) bit is set
gram, a square-wave signal at the fre-
quency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a zero the SQW pin is held low. The state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

**DM** – The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or $\overline{\text{RESET}}$. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data.

**24/12** – The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by software.

**DSE** – The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.

**REGISTER C ($0C)**

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b | b1 | b0 |
|---|---|---|---|---|---|---|---|
| IRQF | PF | AF | UF | 0 | 0 | 0 | 0 |

Read-Only Register

**IRQF** – The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true:

PF = PIE = "1"

AF = AIE = "1"

UF = UIE = "1"

i.e., IRQF = PF•PIE + AF•AIE + UF•UIE

Any time the IRQF bit is a "1", the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

**PF** – The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an $\overline{\text{IRQ}}$ signal and sets the IRQF bit when PIE is also a "1". The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

**AF** – A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the $\overline{\text{IRQ}}$ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1." A $\overline{\text{RESET}}$ or a read of Register C clears AF.

**UF** – The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting $\overline{\text{IRQ}}$. UF is cleared by a Register C read or a $\overline{\text{RESET}}$.

**b3 TO b0** – The unused bits of Status Register 1 are read as "0's". They can not be written.

**REGISTER D ($0D)**

| MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Read Only |
| VRT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Register |

**VRT** — The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read only bit which is not modified by the $\overline{\text{RESET}}$ pin. The VRT bit can only be set by reading Register D.

**b6 TO b0** — The remaining bits of Register D are unused. They cannot be written, but are always read as "0's."

## TYPICAL INTERFACING

The MC146818 is best suited for use with microprocessors which generate an address-then-data multiplexed bus. Figures 17 and 18 show typical interfaces to bus-compatible processors. These interfaces assume that the address decoding can be done quickly. However, if standard metal-gate CMOS gates are used the $\overline{\text{CE}}$ setup time may be violated. Figure 19 illustrates an alternative method of chip selection which will accommodate such slower decoding.

The MC146818 can be interfaced to single-chip microcomputers (MCU) by using eleven port lines as shown in Figure 20. Non-multiplexed bus microprocessors can be interfaced with additional support.

There is one method of using the multiplexed bus MC146818 with non-multiplexed bus processors. The interface uses available bus control signals to multiplex the address and data bus together.

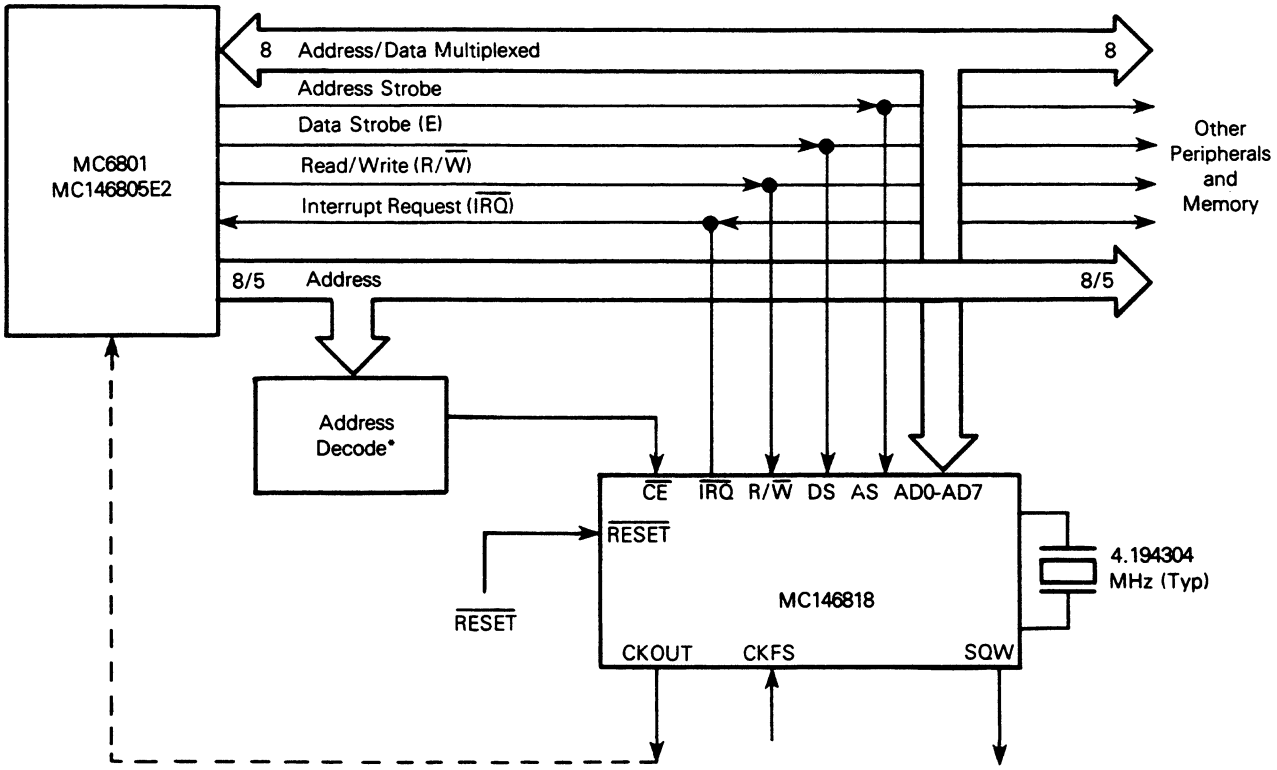
An example using either the Motorola MC6800, MC6802, MC6808, or MC6809 microprocessor is shown in Figure 21.

Figure 22 illustrates the subroutines which may be used for data transfers in a non-multiplexed system. The subroutines should be entered with the registers containing the following data:

Accumulator A: The address of the RTC to be accessed.
Accumulator B: Write: The data to be written.
Read: The data read from the RTC.

The RTC is mapped to two consecutive memory locations — RTC and RTC + 1 as shown in Figure 21.

**FIGURE 17 — MC146818 INTERFACED WITH MOTOROLA COMPATIBLE MULTIPLEXED BUS MICROPROCESSORS**




*High-Speed Silicon-Gate CMOS or TTL Address Decoding

FIGURE 18 — MC146818 INTERFACED WITH
COMPETITOR COMPATIBLE MULTIPLEXED BUS MICROPROCESSORS

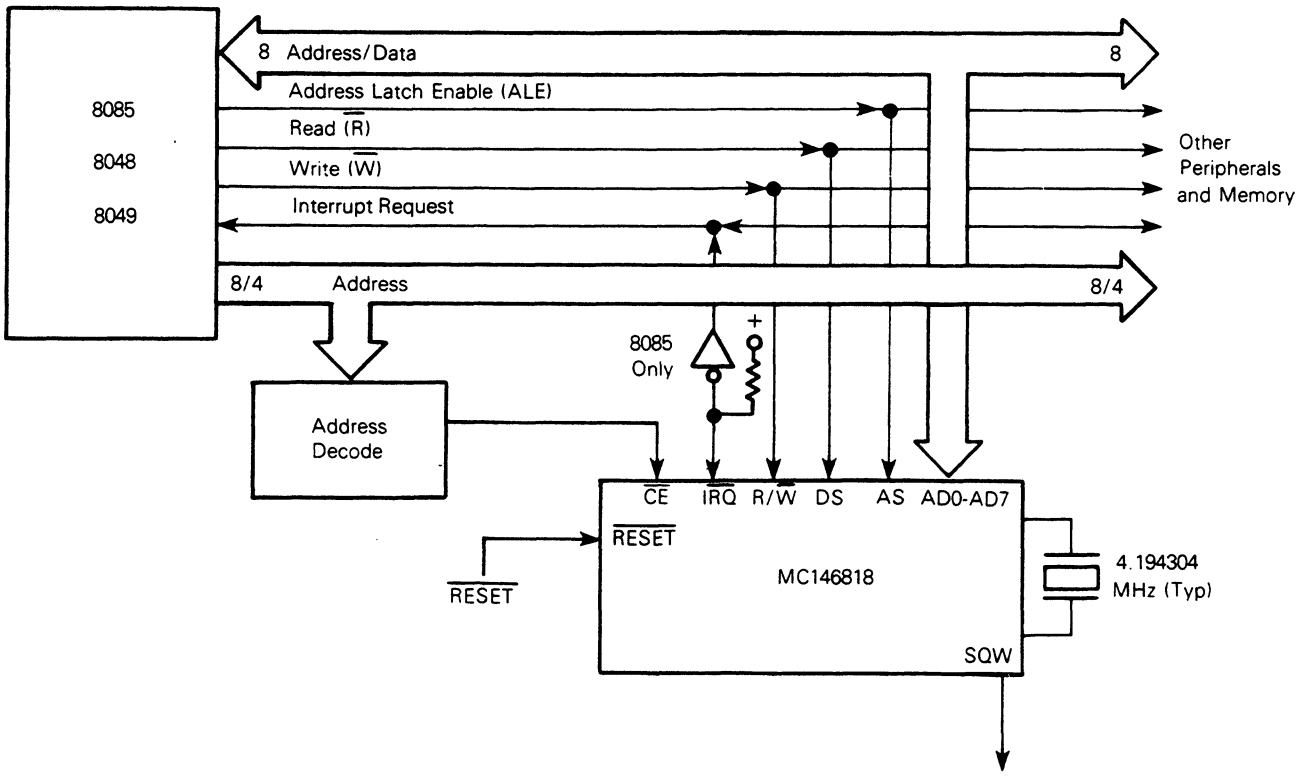
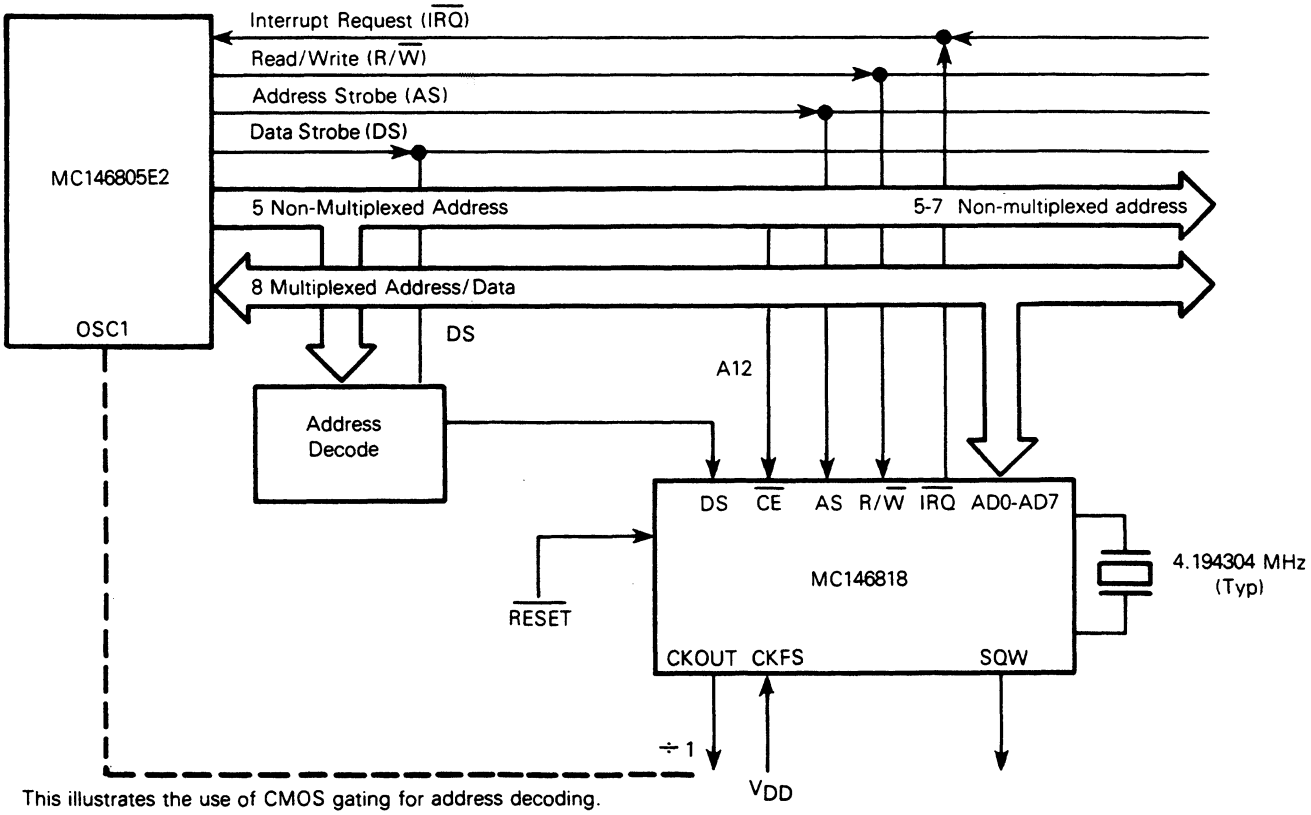



FIGURE 19 — MC146818 INTERFACE WITH MC146805E2
CMOS MULTIPLEXED MICROPROCESSOR WITH SLOW ADDRESSING DECODING




This illustrates the use of CMOS gating for address decoding.

FIGURE 20 — MC146818 INTERFACED WITH THE PORTS OF A TYPICAL SINGLE CHIP MICROCOMPUTER

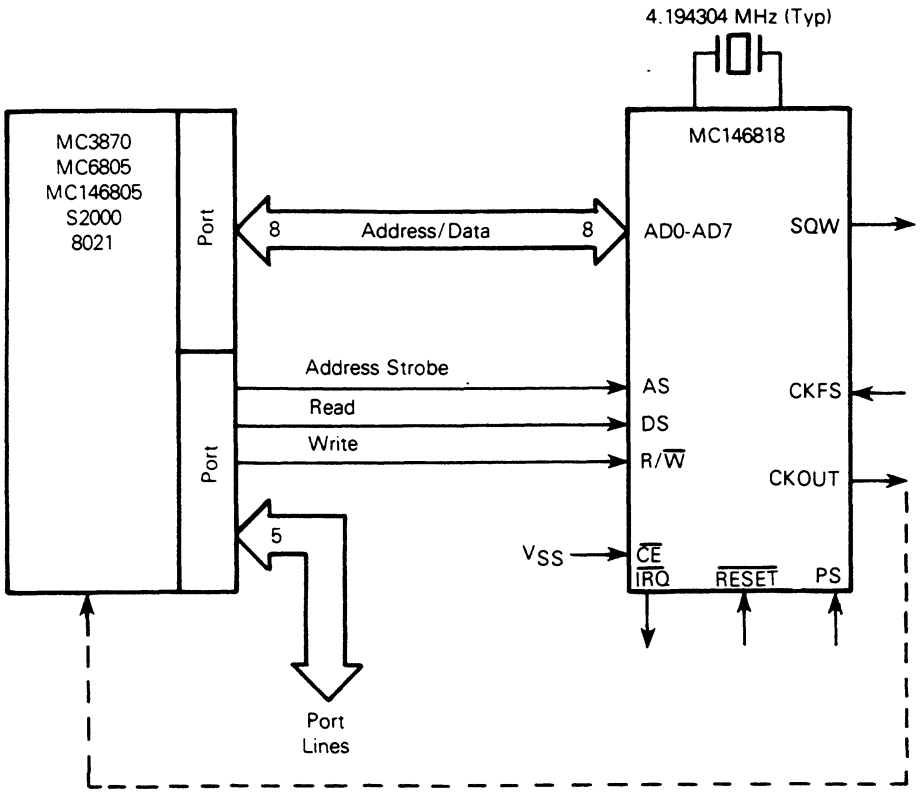



FIGURE 21 — MC146818 INTERFACED WITH MOTOROLA PROCESSORS

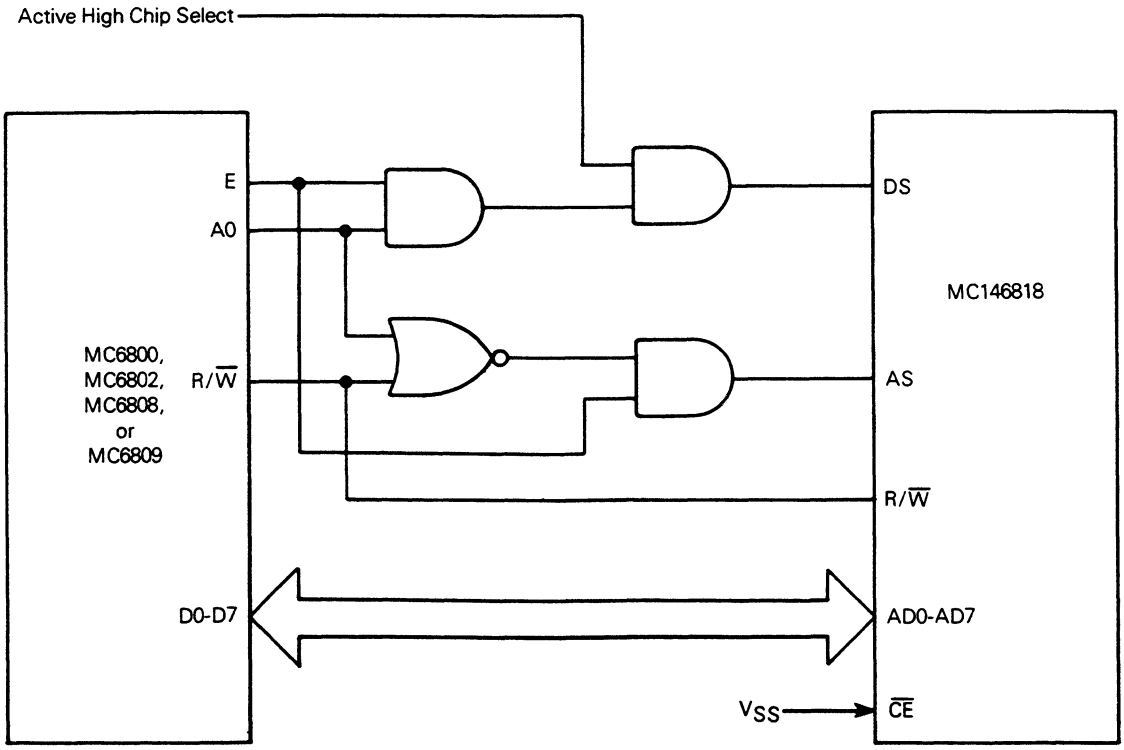


FIGURE 22 — SUBROUTINE FOR READING AND WRITING THE MC146818 WITH A NON-MULTIPLEXED BUS

```
READ    STA     RTC     Generate AS and Latch Data from ACCA
        LDAB    RTC+1   Generate DS and Get Data
        RTS

WRITE   STA     RTC     Generate AS and Latch Data from ACCA
        STAB    RTC+1   Generate DS and Store Data
        RTS
```

## IMPORTANT NOTICES

Those devices made with date code 3N4GXXXX have the following exceptions when used in the Motorola mode of MOTEL.

1. $V_{DD}$ = 3 to 5.25 V for operation
2. DS $V_{IL}$ = 0.6 V Max.

The falling edge of chip select should occur during the active high pulse of address strobe, only on those units with date code GC6XXXX.

| INCHES | |
|---|---|
| MIN | MAX |
| 1.235 | 1.265 |
| 0.540 | 0.560 |
| 0.155 | 0.200 |
| 0.014 | 0.022 |
| 0.040 | 0.060 |
| 0.100 BSC | |
| 0.065 | 0.080 |
| 0.008 | 0.015 |
| 0.115 | 0.135 |
| 0.600 BSC | |
| 0° | 15° |
| 0.020 | 0.040 |

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