Z80 timings on Amstrad CPC - Cheat sheet

This document is a visual layout made by cpcitor/findyway from data at http://www.cpctech.org.uk/docs/instrtim.html / https://cpctech.cpcwiki.de/docs/instrtim.html
Cross-checked with https://borilla.co.uk/z80.html

Instruction timings

The main clock in the CPC is 16Mhz This is provided to the Gate-Array which generates the other clocks.

The Gate Array has the following roles:

generation of a 1Mhz clock for the CRTC and AY-3-8912

generation of a 4Mhz clock for the CPU

arbitrates access to the RAM between the CPU and the video hardware (CRTC and Gate-Array)

Every microsecond:

The CRTC generates a memory address using it's MA and RA signal outputs

The Gate-Array fetches two bytes for each address

The video hardware is given priority so that the display is not disrupted

The Gate-Array generates the "READY" signal which is connected to the "/WAIT" input signal of the CPU. This signal is used to stop the CPU accessing while the video-hardware is accessing it. As a result, all instruction timings are stretched so that they are all multiples of a microsecond (1µs), and this gives an effective CPU clock of 3.3Mhz.

Key:	
cc	condition code (z,nz,c,nc,p,m,po,pe)
r	8-bit register (B,C,D,E,H,L,A)
b	Bit number (0,1,2,3,4,5,6,7)
n	8 bit value
nnnn	16 bit value
dd	8 bit displacement
nc	condition not satisfied
c	condition satisfied

Other timings

Time between acknowledge of a interrupt and execution of a interrupt

Mode 0: (depends on instruction)

Mode 1: 5

Mode 2: 19

1 monitor scanline: 64 microseconds

1 50Hz monitor frame: 19968 microseconds.

NOTES:

(note 1) This timing applies when there are multiple DD or FD prefix's together.

The timings for IY index register pair are identical to the timings for IX register pair.

The table on next page gives the complete execution time for all CPU instructions
"These timings have been measured" (dixit http://www.cpctech.org.uk/docs/instrtim.html)

Credits: CPCWiki community Arnoldemu, Executioner, db6128, TFM, Axelay, Optimus, and the ones I forgot.

V1.1 2013-10-19
V1.2 2022-03-06 clarified special cases of rp
V1.3 2023-07-09 replace rp notation with explicit register list (only omitting IY). Benefit: use your viewer’s search feature for e.g. SP and see all instructions that involve SP at a glance!

ARITHMETIC & LOGIC

1 NOP	2 NOPs	3 NOPs	4 NOPs	5 NOPs	6 NOPs	7 NOPs
ADD A,r ADC A,r SUB r SBC A,r	ADD A,n ADC a,n SUB n SBC A,n ADD A,(HL) ADC A,(HL) SUB A,(HL) SBC A,(HL) ADD A,HIX ADC A,HIX SUB HIX SBC A,HIX	ADD HL,BC ADD HL,DE ADD HL,HL ADD HL,SP	ADD IX,BC ADD IX,DE ADD IX,IX ADD IX,SP ADC HL,BC ADC HL,DE ADC HL,HL ADC HL,SP	ADD A,(IX+dd) ADC A,(IX+dd) SUB (IX+dd) SBC A,(IX+dd) CPD		
AND r XOR r OR r CP r	AND n XOR n OR n CP n AND (HL) XOR (HL) OR (HL) CP (HL) AND HIX XOR HIX OR HIX CP HIX		SBC HL,BC SBC HL,DE SBC HL,HL SBC HL,SP	AND (IX+dd) XOR (IX+dd) OR (IX+dd) CP (IX+dd) CPI		
RLCA RRCA RLA RRA	RLC r RRC r RR r RL r SLA r SLL r SRL r		RLC (HL) RRC (HL) RR (HL) RL (HL) SLA (HL) SLL (HL) SRL (HL)	RLD RRD		RL/RLC (IX+dd) RR/RRC (IX+dd) SLA (IX+dd) SRA (IX+dd) SLL (IX+dd) SRL (IX+dd)

BITS, FLAGS & SPECIAL ARITHMETIC

1 NOP	2 NOPs	3 NOPs	4 NOPs	5 NOPs	6 NOPs	7 NOPs
SCF CCF CPL	BIT b,r RES b,r SET b,r	BIT b,(HL)	RES b,(HL) SET b,(HL)		BIT r,(IX+dd)	RES r,(IX+dd) SET r,(IX+dd)
DAA	NEG					

INCR & DECR

1 NOP	2 NOPs	3 NOPs	4 NOPs	5 NOPs	6 NOPs	7 NOPs
INC r DEC r	INC HL/DE/BC/SP DEC HL/DE/BC/SP INC HIX DEX HIX INC LIX DEC LIX	INC (HL) DEC (HL) INC IX DEC IX			INC (IX+dd) DEC (IX+dd)	

LOAD

1 NOP	2 NOPs	3 NOPs	4 NOPs	5 NOPs	6 NOPs	7 NOPs
LD r,r	LD r,n LD r,HIX LD r,LIX LD HIX,r LD LIX,r	LD BC,nnnn LD DE,nnnn LD HL,nnnn LD SP,nnnn LD HIX,nn LD LIX,nn LD I,A LD A,I LD R,A LD A,R	LD IX,nnnn	LDI LDD	LD (nnnn),BC LD (nnnn),DE LD (nnnn),HL LD (nnnn),SP LD (IX+dd),nn	
	LD r,(HL) LD (HL),r LD A,(BC) LD A,(DE) LD (BC),A LD (DE),A	LD (HL),nn	LD A,(nnnn) LD (nnnn),A	LD (nnnn),HL LD HL,(nnnn) LD r,(IX+dd) LD (IX+dd),r	LD BC,(nnnn) LD DE,(nnnn) LD HL,(nnnn) LD SP,(nnnn) LD (nnnn),IX LD IX,(nnnn)	

LOAD WITH PC a.k.a. JUMP

1 NOP	2 NOPs	3 NOPs	4 NOPs	5 NOPs	6 NOPs	7 NOPs
JP (HL)	JP (IX)	JP nnnn JP cc,nnnn	DJNZ dd b-1=0 : 3, b-1<>0 : 4			
	JR cc,dd nc : 2, c : 3	JR dd RET	RETN RETI			

PUSH/POP/LOAD WITH SP/CALL/RET

1 NOP	2 NOPs	3 NOPs	4 NOPs	5 NOPs	6 NOPs	7 NOPs
		POP AF POP BC POP DE POP HL	PUSH AF PUSH BC PUSH DE PUSH HL	PUSH IX PUSH IY POP IX POP IY		
	LD SP,HL	LD SP,IX	RET cc Nc : 2, c : 4	CALL nnnn CALL cc,nnnn Nc : 3, c : 5	EX (SP),HL	EX (SP),IX

IN/OUT, SPECIAL

1 NOP	2 NOPs	3 NOPs	4 NOPs	5 NOPs	6 NOPs	7 NOPs
NOP HALT EX AF,AF' EX DE,HL EXX, DI, EI DD/FD Prefix (note 1)	ED "nop" (ED 00 - ED 3F) IM 0 IM 1 IM 2	IN A,(nn) OUT (nn),A	IN r,(C) IN F,(C) RST 0 RST 1 RST 2 RST 3 OUT (C),r OUT (C),0 RST 4 RST 5 RST 6 RST 7	OUTI OUTD INI IND	LDIR LDDR CPDR CPIR INDR, INIR OTDR, OTIR Last iteration : BC-1=0 : 5 All others : BC-1<>0 : 6	