131,072 Bit Serial Read Only Memory

FEATURES

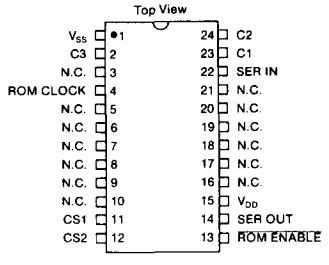
- 16K x 8 Organization
- Single +5 Volt Supply
- Tri-State Serial Output
- Totally Automated Custom Programing
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

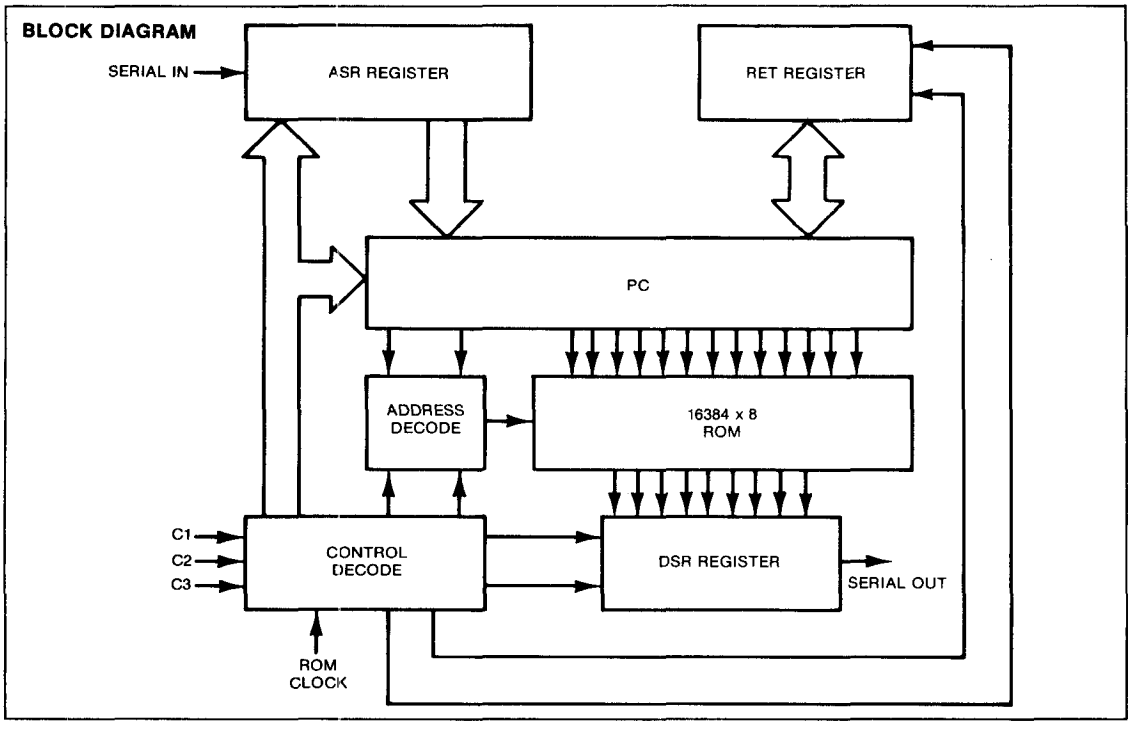
The General Instrument SPR128 is a 131,072 Bit Serial Read Only Memory organized as 16,384 eight-bit words and is ideally suited for interfacing with the SP0256 Speech Processor. Fabricated in the General Instrument advanced N-Channel Ion Implant process to enable operation from a single +5 Volt power supply, up to 4 SPR128s can be interfaced to the SP0256 without buffering.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN ASSIGNMENTS

Pin Number	Name	Function
	$\overline{\text{ROM ENABLE}}$	Active low chip select used in system to eliminate bus conflict at system start-up. When brought high, $\overline{\text{ROM ENABLE}}$ Tri-States Serial Out.
	SERIAL IN	Serial Input used to load 16 bit address into device.
	SERIAL OUT	Output pin used to shift out data byte.
	CS1	Active high chip select. Will Tri-State Serial output when low.
	$\overline{\text{CS2}}$	Active low chip select. Will Tri-State Serial output when high.
	ROM CLOCK	1.56MHz clock input from SP0256 speech processor.
	V_{SS}	Ground pin.
	C3 C2 C1	Control pins decoded to determine device function.
	V_{DD}	Positive supply pin (+4.6V to +7.0V)

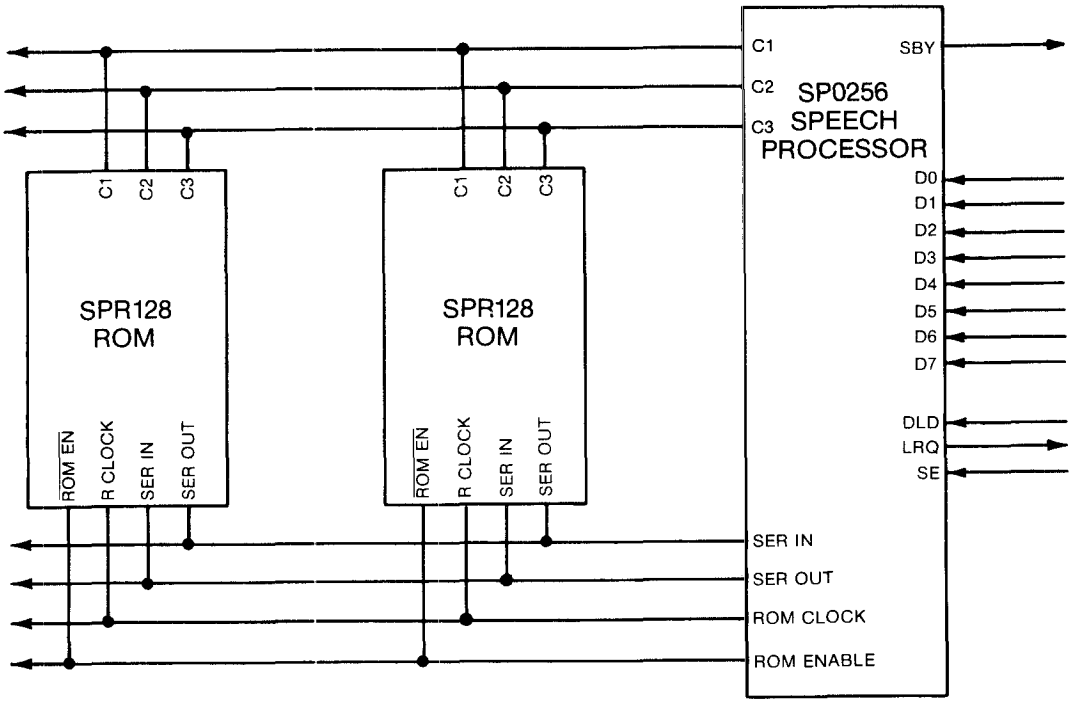


Fig. 1 INTERFACE OF SPR128 ROM TO SP0256 SPEECH PROCESSOR

TABLE 1 SPR128 CONTROL STATES

C1	C2	C3	Function	
0	0	0	**NOP**	No action taken.
0	0	1	**ASR Load**	Accepts data from the serial input, synchronous to the externally supplied ROM clock. This data is shifted into the ASR holding register in preparation for loading into the PC. Although ASR is 16 bits long, it is not necessary to load all 16 bits of address sequentially in one ASR load.
0	1	0	**PC Load**	Loads the contents of the ASR register into the PC.
0	1	1	**DSR Load**	Loads the 8 bits of data pointed to by the present value of the least significant 14 bits of the PC into the data output shift register (DSR). At the completion of the DSR load the PC is incremented.
1	0	0	**DSR Shift-Out**	Shifts out the contents of DSR to the serial out pin, synchronous to the ROM clock.
1	0	1	**RET Register Load**	Loads the return register (RET) with the current value of the PC.
1	1	0	**Return**	Loads the PC with the contents of the RET register.
1	1	1	**NOP**	No action taken.

ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{DD} ..... −.3 to +12V
Storage Temperature ..... −25° to +125°C
Lead Temperature (soldering) 10 Sec ..... +333°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated)

V_{DD} = +4.6V to +7.0V
Operating Temperature = 0°C to +70°C

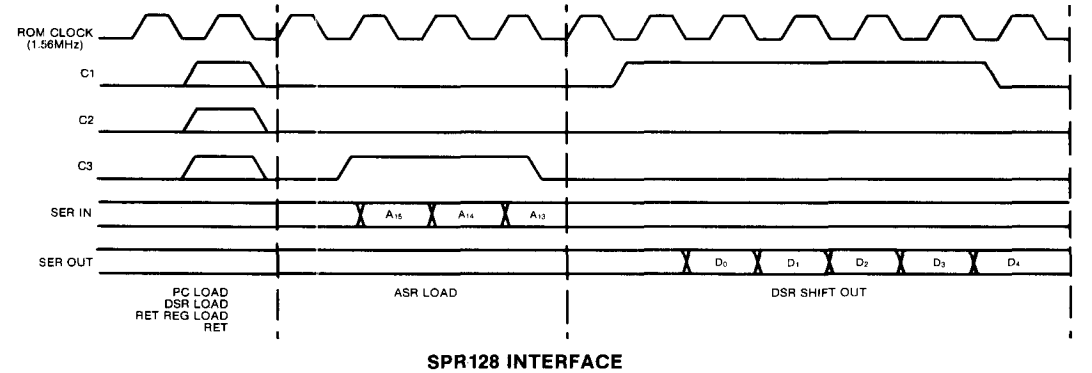
Supply Current

I_{DD} = 25mA V_{DD} = 7.0V ROM clock frequency typically 1.56MHz
V_{SS} = 0.0V T_A = 0°C

DC CHARACTERISTICS

Characteristics	Sym	Min	Max	Units	Conditions
Inputs					
$\overline{\text{ROM ENABLE}}$, SERIAL IN, CS1, $\overline{\text{CS2}}$, C1, C2, C3					
ROM Clock					
Logic 0	V_{IL}	0	0.6	V	
Logic 1	V_{IH}	2.4	V_{DD}	V	
Capacitance	C_{IN}	—	10	pf	
Leakage	C_{IN}	—	10	μA	V Pin = V_{DD} Volts, all others grounded
Outputs					
SERIAL OUT					
Logic 0	V_{OL}	0	0.6	V	I_L = 1.6mA
Logic 1	V_{OH}	2.5	V_{DD}	V	I_L = −50μA
Leakage	I_{LO}	—	10	μA	Output Tristated

TIMING DIAGRAM



SPR128 INTERFACE