VL6845R/E • VL68C45R/S

VL6845 CRT CONTROLLER FAMILY AND VMC68C45 MEGACELL DESIGN KIT

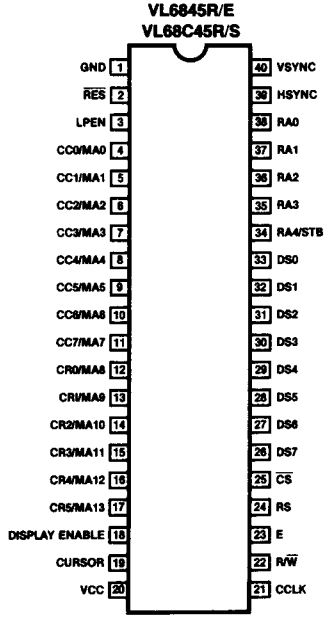
FEATURES

- CRT Controller Family—
  Rev E compatibility with SY6845E
  Rev R compatibility with MC6845
  CMOS versions available:
  CMOS Rev R compatible with MC6845R1, MC6845 and MC146845 CMOS Rev S compatible with HD6845S
- Internal refresh address generation
- Character clocks up to 5 MHz
- Bus clocks up to 3 MHz

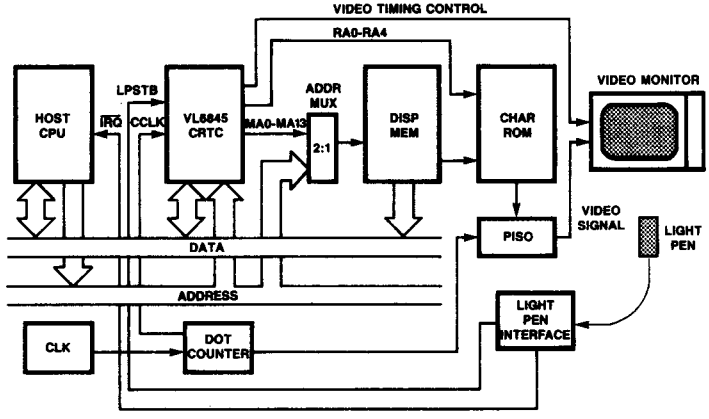
DESCRIPTION

The VL6845X and VL68C45X are a family of CRT controllers that are widely used in both bit-mapped and character-mapped applications for both terminals and personal computers. The VL6845 family offers compatibility with the Motorola family of HMOS controllers while the VL68C45 family allows designs to consume less power through the use of CMOS technology. In addition to compatibility with both the Motorola and Hitachi families, the VL68C45R also contains enhancements found in the MC6845R1. These enhancements allow for higher resolution displays without extra external hardware.

PIN DIAGRAM



SYSTEM DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency		Part Number	Clock Frequency		Package
	Bus	Character		Bus	Character	
VL6845R-23 VL68C45R-23 VL68C45S-23	2 MHz	3 MHz	VL6845E-33 VL6845R-33 VL68C45R-33 VL68C45S-33	3 MHz	3 MHz	To specify package type, add the appropriate suffix to the part number: PC = Plastic DIP CC = Ceramic DIP QC = Plastic Leaded Chip Carrier (PLCC)
VL6845E-24 VL6845R-24 VL68C45R-24 VL68C45S-24		4 MHz	VL6845E-34 VL6845R-34 VL68C45R-34 VL68C45S-34		4 MHz	
			VL6845R-35 VL68C45R-35 VL68C45S-35		5 MHz	

Note: Operating temperature range: 0°C to +70°C.

PIN DESCRIPTIONS

Pin	Pin Number	Pin Name	Description
MPU Interface			
E	23	Enable	Input that is used as a data strobe; does not have to be a free-running clock. This capability allows the VL6845 to interface with other non-6800/6500-type microprocessors.
R/$\overline{W}$	22	Read/$\overline{\text{Write}}$ Control	Input that, when HIGH, allows the processor to read the data supplied by the VL6845; when this signal is LOW, the processor writes into the VL6845.
$\overline{CS}$	25	$\overline{\text{Chip Select}}$	Input that, when HIGH, deselects VL6845; when this signal is LOW, the VL6845 is selected. This signal is typically connected to the system address bus either directly or through an address decoder.
RS	24	Register Select	Input that, when LOW, selects the Address Register of the VL6845 for a write operation. When this signal is HIGH, an internal register of the VL6845 specified by the contents of the address register is selected.
D0-D7	26-33	Data Bus	Eight bidirectional data lines that are used for transferring data between the microprocessor and the VL6845. These lines are normally high-impedance, except during read and write cycles when the chip is selected.
Video Memory Character Generator Interface			
CC0/MA0-CC5/MA13	4-17	Video Memory Address	Active-HIGH output signals that are used to address the video display memory in binary addressing mode. These memory addresses are generated in a binary sequential fashion. In row/column addressing mode, MA0-MA7 function as column addresses, and MA8-MA13 function as row addresses.
RA0-RA4/STB	34-38	Raster Address	Active-HIGH output signals that are used as address lines to the external character generator ROM. In the transparent addressing mode, RA4 functions as an active-HIGH output strobe.
HSYNC	39	Horizontal Sync	Active-HIGH, TTL-compatible output signal that is used to determine the horizontal position of the displayed text. HSYNC may drive a CRT monitor directly or may be used for composite video generation. Position and width of HSYNC width are fully programmable.
VSYNC	40	Vertical Sync	Active-HIGH, TTL-compatible output signal that is used to determine the vertical position of the displayed text. VSYNC may be used to drive a CRT monitor directly or may be used for composite video generation. VSYNC position is fully programmable.
DISPLAY	18	Display Enable	TTL-compatible output that, when HIGH, indicates that the VL6845 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed rows are both fully programmable and together are used to generate the Display Enable signal.
CURSOR	19	Cursor	TTL-compatible output that when HIGH, indicates a valid cursor address to the external video processing logic.
LPSTB	3	Light Pen Strobe	HIGH-impedance, edge-sensitive input signal that latches the current refresh address into the light pen register. Latching occurs on the LOW-to-HIGH transition edge.
CCLK	21	Character Clock	Input signals derived from the external dot clock, that is used as the time base for all internal count and control functions.
$\overline{RES}$	2	$\overline{\text{Reset}}$	Input signal that when LOW, resets all internal counters. All scan and video outputs are LOW and all control registers are unaffected. RES can be used to synchronize display frame timing with the line frequency.
VCC	20	Supply Voltage	5 V supply
GND	1	Ground	Supply and signal ground

VL6845 FAMILY FUNCTIONAL DESCRIPTION

The VL6845 CRT Controller (CRTC) consists of programmable horizontal and vertical timing generators, programmable linear address registers, programmable cursor logic, a light pen capture register and control circuitry for interface to a processor bus.

All CRTC timing is derived from the character clock (CCLK), which is usually the output of an external dot rate counter. Coincidence circuits internal to the chip continuously compare counter contents to the programmed register file (R0-R17) for generation of Horizontal Sync, Vertical Sync, Display Enable, Cursor and other signals required to interface to a CRT display.

The linear address generator is also driven by the CCLK and locates the positions of characters in memory with respect to their positions on the screen. Fourteen address lines, MA0-MA13 are available for addressing up to 16K characters of memory. The CRTC addresses the memory in the binary sequential fashion. Using the start address register, hardware scrolling through the 16K character memory is possible. The linear address generator continues to increment during the horizontal and blanking periods, so memory refresh can be performed during the blanking periods. The linear address generator repeats the same sequence of addresses for each scan line of a character row. Although the linear address generator continues to increment during the horizontal and blanking periods, the correct address for the first displayed character or row is always maintained.

The Cursor logic determines the cursor location, size and blink rate on the screen.

The Light Pen Strobe latches the current contents of the address counter into the light pen register on LOW-to-HIGH transition.

INTERLACE MODE SELECTION

In the normal sync mode (non-interlace), only one field is available, as shown in Figure 1a. Each scan line is refreshed at the VSYNC frequency (50 or 60 Hz).

Two interlace modes are available as shown in Figure 1b and Figure 1c. The frame time is divided between even and odd alternating fields. The horizontal and vertical timing relationship (VSYNC delayed by one-half scan line time) results in the displacement of scan lines in the odd field with respect to the even field.

In the interlace sync mode, the same information is painted in both fields, as shown in Figure 1b. This is a useful mode for filling in a character to enhance readability.

In the interlace sync and video mode, as shown in Figure 1c, alternating lines of the character are displayed in the even field and the odd field. This effectively doubles the given band width of the CRT monitor.

Care must be taken when using either interlace mode to avoid an apparent flicker effect. This flicker effect is due to the doubling of the refresh time for all scan lines since each field is displayed alternately and may be minimized with proper monitor design i.e., longer persistence phosphors.

VL6845R/VL68C45R REGISTER FILE DESCRIPTIONS

The 19 registers of the CRTC may be accessed through the data bus. Only two memory locations are required, as one location is used as a pointer to address one of the remaining 18 registers. These 18 registers control horizontal timing, vertical timing, interlace operation and row address operation. They also define the cursor, cursor address, start address and light pen register. The register addresses and sizes are shown in Table 1.

ADDRESS REGISTER (AR)

The Address Register is a 5-bit write-only register used as an "indirect" or "pointer" register. It contains the address of one of the other 18 registers. When both RS and $\overline{CS}$ are LOW, the Address Register is selected. When $\overline{CS}$ is LOW and RS is HIGH, the register pointed to by the address register is selected.

FIGURE 1a.
NORMAL SYNC

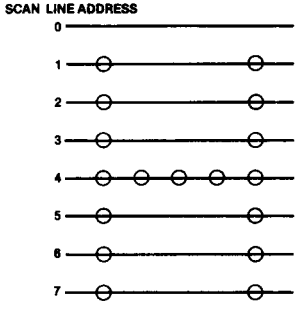


FIGURE 1b.
INTERLACE SYNC

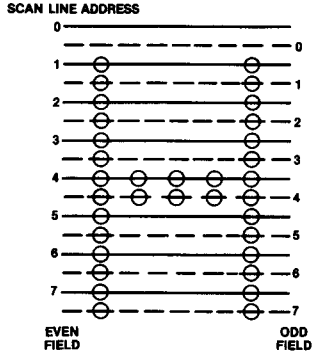
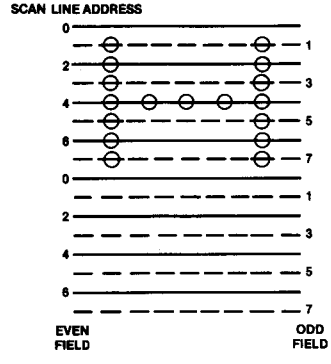


FIGURE 1c.
INTERLACE SYNC AND VIDEO



VL6845R/VL68C45R REGISTER FILE DESCRIPTIONS (Cont.)

HORIZONTAL TOTAL REGISTER (R0)

This 8-bit write-only register determines the horizontal sync (HSYNC) frequency by defining the HSYNC period in character times. It is the total of the displayed characters plus the non-displayed character times (retrace) minus one.

HORIZONTAL DISPLAYED REGISTER (R1)

This 8-bit write-only register determines the number of displayed characters per line. Any 8-bit number may be programmed as long as the contents of R0 are greater than the contents of R1.

HORIZONTAL SYNC POSITION REGISTER (R2)

This 8-bit write-only register controls the HSYNC position, which defines the horizontal sync delay (front porch) and the horizontal scan delay (back porch). When the programmed value of this register is increased, the display on the CRT screen is shifted to the left. When the programmed value is decreased, the display is shifted tot he right. Any 8-bit number may be programmed as long as the sum of the contents of R2 and R3 is less than the contents of R0. The contents of R2 must be greater than R1.

SYNC WIDTH REGISTER (R3)

This 8-bit write-only register determines the width of the HSYNC pulse. The vertical sync pulse width is fixed at 16 scan-line times. HSYNC pulse width may be programmed from 1 to 15 character clock periods, thus allowing compatibility with the HSYNC pulse width specifications of many different monitors. If zero is written into this register, no horizontal sync is provided.

HORIZONTAL TIMING SUMMARY

The difference between R0 and R1 is the horizontal blanking interval. This interval in the horizontal scan period allows the beam to return (retrace) to the left side of the screen. The retrace time is determined by the monitor horizontal scan components. Retrace time is less than the horizontal blanking interval.

A good rule of thumb is to make the horizontal blanking about 20% of the total horizontal scanning period for a CRT. In inexpensive TV receivers the beam over-scans the display screen so that aging of parts does not result in underscanning. Because of this, the retrace time should be about one-third the horizontal scanning period. The horizontal sync delay is typically programmed with a 1:2:2 ratio.

VERTICAL TOTAL REGISTER (R4) AND VERTICAL TOTAL ADJUST REGISTER (R5)

The vertical sync (VSYNC) frequency is determined by both R4 and R5. The

TABLE 1: VL6845R/VL68C45R INTERNAL REGISTER ASSIGNMENTS

$\overline{CS}$	RS	Address Register					Register #	Register File	Program Unit	Read	Write	Number of Bits							
		4	3	2	1	0						7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	—	—	—	—								
0	0	X	X	X	X	X	AR	Address Register	—	No	Yes								
0	1	0	0	0	0	0	RO	Horizontal Total	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes					H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position	Char. Row	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes							I	I
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes		B	P				(Note 2)	
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)	—	No	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	—	No	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	—	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	—	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	—	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	—	Yes	No								

Notes:

1. The interlace bits are described in Table 2.
2. Bit 5 of the cursor start raster register is used for blink period, control, and bit 6 is used to select blink or no-blink.
3. Registers R4, R6 and R7 in the VL68C45R are eight bits wide, instead of seven, for compatibility with the Motorola 6845R1.

VL6845R/VL68C45R REGISTER FILE DESCRIPTIONS (Cont.)

calculated number of character row times is usually an integer plus a fraction to get exactly a 50 Hz or 60 Hz vertical refresh rate. The integer number of character row times minus one is programmed into the 7-bit write-only vertical total register (R4). The fraction of character line times is programmed into the 5-bit write-only vertical total adjust register (R5) as the number of scan lines required.

VERTICAL DISPLAYED REGISTER (R6)

This 7-bit write-only register specifies the number of character rows displayed on the CRT screen, and is programmed in character row times. Any number smaller than contents R$ may be programmed into R6.

VERTICAL SYNC POSITION REGISTER (R7)

This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. When programmed value of this register is increased, the display position of the CRT screen is shifted up. When the programmed value is decreased, the display position is shifted down. Any number equal to or less than the contents of R4 and greater than or equal to the R6 may be used.

INTERLACE MODE AND SKEW REGISTER (R8)

The VL6845R only allows control of the interlace modes as programmed by the low-order two bits of this write-only register. Table 2 shows the interlace modes available to the user. These modes are selected using the two low order bits of this 6-bit write-only register.

TABLE 2: INTERLACE MODE REGISTER

Bit 1	Bit 2	Mode
0	0	Normal Sync Mode
1	0	(Non-interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

INTERLACE MODE AND SKEW REGISTER (R8) (Cont.)

There are restrictions on the programming of the VL6845R/VL68C45R registers for interlace operation:

1. The Horizontal Total Register (R0) value must be odd (i.e., and even number of character times).
2. For interlace sync and video mode only, the Maximum Scanline Address Register (R9) value must be odd (i.e., an even number of scan lines).
3. For interlace sync and video mode only, the number (Nvd) programmed into the Vertical Display Register (R6) must be one-half the actual number required. The even-numbered scan lines are displayed in the even field and the odd-numbered scan lines are displayed in the odd field.
4. For interlace sync and video mode only, the Cursor Start Register (R10) and Cursor End Register (R11) must both be even or odd, depending on which field the cursor is to be displayed in. A full block cursor will be displayed in both in both the even and the odd field when the Cursor End Register (R11) is programmed to a value greater than the value in the Maximum Scan Line Address Register (R9).

MAXIMUM SCAN LINE ADDRESS REGISTER (R9)

This 5-bit write-only register determines the number of scan lines per character row, including the spacing, thus controlling operation of the row address counter. The programmed value is a maximum address and is one less than the number of scan lines.

CURSOR CONTROL REGISTERS

CURSOR START REGISTER (R10) AND CURSOR END REGISTER (R11)

These registers allow a cursor of up to 32 lines in height to be placed on any scan line of the character block. Register R10 is a 7-bit write-only register used to define the start scan line and the cursor blink rate. Bits 5 and 6 of the Cursor Start Address Register control the cursor operation as shown in table 3. Non-display, display, and two blink modes (16 times or 32 times the field period) are available. Register R11 is a 5-bit write-only register that defines the last scan cursor.

TABLE 3: CURSOR START REGISTER

Bit 6	Bit 5	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink, 1/16 field rate
1	1	Blink, 1/32 field rate

When an external blink feature on characters is required, it may be necessary to perform cursor blink externally so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRT for a blinking cursor and externally inverting the video signal with an exclusive-OR gate.

CURSOR REGISTER (R14-H, R15-L)

This 14-bit read/write register pair is programmed to position the cursor anywhere in the refresh RAM area, thus allowing hardware paging and scrolling through memory without loss of the original cursor position. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register.

START ADDRESS AND LIGHT PEN REGISTERS

START ADDRESS REGISTER (R12-H, R13-L)

This 14-bit write-only register pair controls the first address output by the CRTC after vertical blanking. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register. The start address register determines which portion of the refresh RAM is displayed on the CRT screen. Hardware scrolling by character or page may be accomplished by modifying the contents of this register.

LIGHT PEN REGISTER (R16-H, R17-L)

This 14-bit read-only register pair captures the refresh address output by the CRTC on the positive edge of a pulse input to the LPSTB pin. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register. Since the light pen pulse is asynchronous with respect to refresh address timing, an internal synchronizer is designed into the CRTC. Due to delays in this circuit, the value of R16 and R17 will need to be corrected in software. (See the bus timing diagram in the Timing Characteristics section.)

VL68C45S
REGISTER FILE DESCRIPTIONS

TABLE 4: VL68C45S INTERNAL REGISTER ASSIGNMENTS, Note 1

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register Name	Program Unit	READ	WRITE	Data Bit 7	6	5	4	3	2	1	0
1	x	x	x	x	x	x			–	–	–								
0	0	x	x	x	x	x	AR	Address Register	–	×	○								
0	1	0	0	0	0	0	R0	Horizontal Total*	Character	×	○								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Character	×	○								
0	1	0	0	0	1	0	R2	Horizontal Sync* Position	Character	×	○								
0	1	0	0	0	1	1	R3	Sync Width	Vertical-Raster, Horizontal-Character	×	○	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0	0	1	0	0	R4	Vertical Total*	Line	×	○								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	Raster	×	○								
0	1	0	0	1	1	0	R6	Vertical Displayed	Line	×	○								
0	1	0	0	1	1	1	R7	Vertical Sync* Position	Line	×	○								
0	1	0	1	0	0	0	R8	Interlace & Skew	–	×	○	C1	C0	D1	D0			V	S
0	1	0	1	0	0	1	R9	Maximum Raster Address	Raster	×	○								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Raster	×	○		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Raster	×	○								
0	1	0	1	1	0	0	R12	Start Address (H)	–	○	○								
0	1	0	1	1	0	1	R13	Start Address (L)	–	○	○								
0	1	0	1	1	1	0	R14	Cursor (H)	–	○	○								
0	1	0	1	1	1	1	R15	Cursor (L)	–	○	○								
0	1	1	0	0	0	0	R16	Light Pen (H)	–	○	×								
0	1	1	0	0	0	1	R17	Light Pen (L)	–	○	×								

Note:
1. ○ = yes; × = no

VL68C45S REGISTER FILE DESCRIPTIONS (Cont.)

ADDRESS REGISTER (AR)

This is a 5-bit register that is used to select 18 internal control registers (R0-R17). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0-R17 requires writing the address of the corresponding control register into this register. When RS and CS are LOW, the address is selected.

HORIZONTAL TOTAL REGISTER (R0)

This 8-bit register is used to program the total number of horizontal characters per line, including the retrace period. The data value should be programmed according to the specification of the CRT. When M is the total number of characters, (M-1) must be programmed into this register. When programming for interlace mode, M must be even.

HORIZONTAL DISPLAYED REGISTER (R1)

This 8-bit register is used to program the number of horizontal displayed characters per line. Any 8-bit number that is smaller than that of horizontal total register contents can be programmed.

HORIZONTAL SYNC POSITION REGISTER (R2)

This 8-bit register is used to program horizontal sync position as multiples of the character clock period. Any 8-bit number that is lower than the horizontal total register contents can be programmed. When H is the character number of the horizontal sync position, (H-1) must be programmed into this register. When the programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When the programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

SYNC WIDTH REGISTER (R3)

This 8-bit register is used to program the horizontal sync (HS) pulse width and the vertical sync (VS) pulse width. The horizontal sync pulse width is programmed in the lower four-bits as multiples of the character clock period (see Table 5); a zero cannot be programmed. The vertical sync pulse width is programmed in the higher four bits as multiples of the raster period (see Table 6). When zeroes are programmed in the higher four bits, a 16-raster period is specified.

VERTICAL TOTAL REGISTER (R4)

This 7-bit register is used to program the total number of lines per frame, including vertical retrace period. The data and its value should be programmed according to the specification of the CRTC. When N is the total number of lines, (N-1) must be programmed into this register.

VERTICAL TOTAL ADJUST REGISTER (R5)

This 5-bit register is used to program the optimum number to adjust the total number of rasters per field. This register enables more precise control of the deflection frequency.

VERTICAL DISPLAYED REGISTER (R6)

This 7-bit register is used to program the number of displayed character rows on the CRT screen. Any 7-bit number that is smaller than that of vertical total register contents can be programmed.

VERTICAL SYNC POSITION REGISTER (R7)

This 7-bit register is used to program the vertical sync position on the screen as multiples of the horizontal character line period. Any number that is equal to or less than the vertical total register content can be programmed. When V is the character number of vertical sync position, (V-1) must be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When the programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

INTERLACE AND SKEW REGISTER (R8)

This register is used to program raster scan mode and skew (delay) of the Cursor signal and Display Enable signals.

INTERLACE MODE PROGRAM BITS (V,S)

Raster scan mode is programmed (see Table 7) by the V and S bits of R8. In the non-interlace mode, duplicate scanning is done of the rasters of even number field and odd number field. In the interlace sync mode, the rasters of the odd number field are scanned in the middle of the even number field. The same character pattern is then displayed in two fields. In the interlace sync and video mode, the raster scan method is the same as in the interlace sync mode, but it is controlled to display different character patterns in two fields.

Note:

1. The registers marked *:
   (written value) = (specified value) − 1
2. Written value of R9:
   a) Non-interlace mode and Interlace Sync Mode (written value Nr) = (specified value) − 1
   b) Interlace sync and video mode: (Written value Nr) = (specified value) − 2
3. CO and C1 specify skew of CURSOR output signal.
   DO and D1 specify skew of Display Enable output signal. When S is one, V specifies video mode. S specifies the Interlace sync mode.
4. B specifies cursor blink.
   P specifies the cursor blink period.
5. wv0~wv3 specify the pulse width of the vertical sync signal. wh0~wh3 specify the pulse width of the horizontal sync signal.
6. RO is normally programmed to be an odd number in interlace mode.
7. 0 = Yes, X = No

VL68C45S
REGISTER FILE DESCRIPTIONS (Cont.)

TABLE 5: PULSE WIDTH OF HORIZONTAL SYNC SIGNAL

VSW/HSW Register (R3)				HSW Pulse Width (multiples of char clock period)
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	Not Allowed
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

TABLE 6: PULSE WIDTH OF VERTICAL SYNC SIGNAL

VSW/HSW Register (R3)				VSW Pulse Width (multiples of raster period)
Bit 7	Bit 6	Bit 5	Bit 4	
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

TABLE 7: INTERLACE MODE BITS (BITS 1 AND 0 of R8)

V Bit 1	S Bit 2	Mode
0	0	Normal Sync Mode
1	0	(Non-interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

SKEW PROGRAM BITS (C1,C0,D1,D0)

These bits are used to program the skew (delay) of the Cursor and Display Enable signals.

Skew of these two kinds of signals is programmed separately. The skew function is used to provide an on-chip delay for the output timing of the of the Cursor and Display Enable signals to provide the time required to access refresh memory, character generator or pattern generator, and to ensure that they are in phase with the serial video signal.

TABLE 8: DISPLAY ENABLE SKEW BIT (BITS 5 AND 4 OF R8)

D1 Bit 5	D0 Bit 4	Display Enable Signal
0	0	Non-Skew
0	1	One-character Skew
1	0	Two-character Skew
1	1	Non-output

TABLE 9: CURSOR SKEW BITS (BITS 7 & 6 OF R8)

C1 Bit 7	C0 Bit 6	Display Skew
0	0	Non-Skew
0	1	One-character Skew
1	0	Two-character Skew
1	1	Non-output

VL68C45S REGISTER FILE DESCRIPTIONS (Cont.)

MAXIMUM RASTER ADDRESS REGISTER (R9)

This 5-bit register is used to program the Maximum Raster Address. This register defines total number of rasters per character, including space.

This register is programmed as follows:

1. Non-Interlace Mode,
   Interlace Sync Mode:
   When the total number of rasters is RN, (RN-1) must be programmed.
2. Interlace Sync and Video Mode:
   When total number of rasters is RN, (RN-2) must be programmed.

The total number of rasters in non-interlace mode, interlace sync mode and interlace sync and video mode is defined as follows in Table 10.

TABLE 10: RASTER COUNT IN INTERLACE AND NON-INTERLACE MODES

0 _____ Total number of rasters 5
1 _____ Programmed value Nr = 4
2 _____ (The same as displayed total number of rasters)
3 _____
4 _____
Raster Address

INTERLACE SYNC MODE

0 _____ Total number of rasters 5
_ _ _ _ _ _ _ _ _ _ _ 0 programmed value Nr = 4
1 _____
_ _ _ _ _ _ _ _ _ _ _ 1
2 _____
_ _ _ _ _ _ _ _ _ _ _ 2
3 _____
_ _ _ _ _ _ _ _ _ _ _ 3
4 _____
_ _ _ _ _ _ _ _ _ _ _ 4
In the interlace sync mode, total number of rasters in both the even and odd fields is ten. On programming, the half of it is defined as total number of rasters.
Raster Address

INTERLACE SYNC AND VIDEO MODE

0 _____ Total Number of Rasters 5
_ _ _ _ _ _ _ _ _ _ _ 1 Programmed Value Nr = 3
2 _____
_ _ _ _ _ _ _ _ _ _ _ 3
4 _____
(Total number of rasters displayed in the even field and the odd field)
Raster Address

Note:
1. In the interlace mode, pulse width is changed + ½ raster time when vertical sync signal extends over two fields.

CURSOR START RASTER REGISTER (R10)

This 7-bit register is used to program the cursor start raster address and the cursor display mode. The lower five bits program the raster address and the higher two bits program the display mode (see table 11).

TABLE 11: CURSOR DISPLAY MODE (BITS 6 AND 5 OF R10)

B Bit 6	P Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate

Note:
The blink sequence is follows:

Light	Dark

(16 x or 32 x the field period)

CURSOR END RASTER REGISTER (R11)

This register is used to program the cursor end raster address.

START ADDRESS REGISTER (R12, R13)

This register pair is used to program the first address of refresh memory read out. Paging and scrolling are easily performed using this register. This register can be read but the higher 2-bits of R12 are always zero.

CURSOR REGISTER (R14,R15)

These two read/write registers store the cursor location. The higher 2 bits of R14 are zero.

LIGHT PEN REGISTER (R16,R17)

These read-only registers are used to capture the detection address of the light pen. The higher 2 bits of R16 are always zero. The value of R16 and R17 needs to be corrected by software because there is a time delay from the address output by the CRTC to the signal input to its LPSTB pin that the light pen detects.

CONSIDERATIONS IN UPDATING REGISTERS

The value programmed into the internal registers directly controls the CRT. Consequently, the display may flicker on the screen when the contents of the registers are changed from the bus side asynchronously with display operation.

RESTRICTIONS ON PROGRAMMING INTERNAL REGISTERS

1. $0 \leq Nhd \leq Nht + 1 \leq 256$
2. $0 \leq Nvd \leq Nvt + 1 \leq 128$
3. $0 \leq Nhsp \leq Nht$
4. $0 \leq Nvsp \leq Nvt$, Note 1
5. $0 \leq NCSTART \leq NCEND \leq Nr$ (non-interlace, interlace sync mode)
   $0, NCSTART \leq NCEND \leq Nr + 1$ (interlace sync and video mode)
6. $2 \leq Nr \leq 30$
7. $3 \leq Nht$ (except non-interlace mode)
   $5 \leq Nht$(non-interlace mode only)

UPDATING THE CURSOR REGISTER

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace periods.

UPDATING THE START ADDRESS REGISTER

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display periods.

It is desirable to avoid programming any registers besides the cursor and Start Address Register during display operations.

VL6845E
REGISTER FILE DESCRIPTIONS

TABLE 12: VL6845E INTERNAL REGISTER ASSIGNMENT

		Address Register										Register Bit							
$\overline{CS}$	RS	4	3	2	1	0	Register Number	Register Name	Stored Info.	RD	WR	7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Register	Register Number		√				A4	A3	A2	A1	A0
0	0	–	–	–	–	–	–	Status Register		√		U	L	V					
0	1	0	0	0	0	0	R0	Horizontal Total	# Character-1		√								
0	1	0	0	0	0	1	R1	Horizontal Displayed	# Character		√								
0	1	0	0	0	1	0	R2	Horizontal Sync Position	# Character		√								
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Character TImes		√	V3	V2	V1	V0	H3	H2	H1	H0
0	1	0	0	1	0	0	R4	Vertical Total	# Character Row -1		√								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	# Scan Lines		√								
0	1	0	0	1	1	0	R6	Vertical Displayed	# Character Rows		√								
0	1	0	0	1	1	1	R7	Vertical Sync Position	# Character Rows		√								
0	1	0	1	0	0	0	R8	Mode Control			√	U1	U0	C	D	T	RC	I1	I0
0	1	0	1	0	0	1	R9	Scan Line	# Scan Lines -1		√								
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B1	B0					
0	1	0	1	0	1	1	R11	Cursor End	Scan Line Number		√								
0	1	0	1	1	0	0	R12	Display Start Addr (H)	Row		√								
0	1	0	1	1	0	1	R13	Display Start Addr (L)	Column		√								
0	1	0	1	1	1	0	R14	Cursor Position (H)	Row	√	√								
0	1	0	1	1	1	1	R15	Cursor Position (L)	Column	√	√								
0	1	1	0	0	0	0	R16	Light Pen Register (H)		√									
0	1	1	0	0	0	1	R17	Light Pen Register (L)		√									
0	1	1	0	0	1	0	R18	Update Location (H)			√								
0	1	1	0	0	1	1	R19	Update Location (L)			√								
0	1	1	1	1	1	1	R31	Dummy Location											

Note:

1. ▒ designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = "1" which operates likewise.

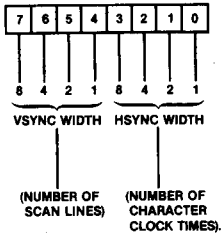
VL6845E REGISTER FILE DESCRIPTIONS (Cont.)

ADDRESS REGISTER

This 5-bit register is used as a "pointer" to direct VL6845E data transfers to and from the system MPU. Its contents are the number of the desired register (0-31). When RS is LOW, the address register may be loaded; when RS is HIGH, the register selected is the one whose identity is stored in this register.

STATUS REGISTER

This 3-bit register is used to monitor the status of the CRTC. It is only accessed in reading, while the Address Register is only accessed in writing. Both these registers are accessed with RS and $\overline{CS}$ LOW.



*IF BITS 4-7 ARE ALL "0" THEN VSYNC WILL BE 16 SCAN LINES WIDE.

HORIZONTAL TOTAL REGISTER (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The horizontal sync (HSYNC) frequency is thus determined by this register.

HORIZONTAL DISPLAYED REGISTER (R1)

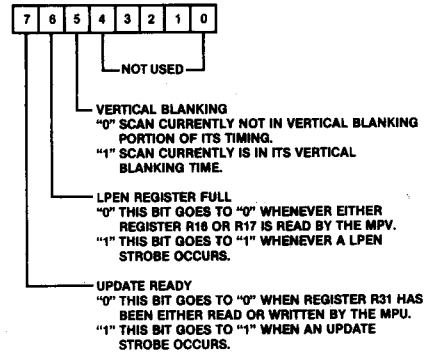
This 8-bit register contains the number of displayed characters per horizontal line.

HORIZONTAL SYNC POSITON REGISTER (R2)

This 8-bit register contains the HSYNC position on the horizontal line, in terms of the character location number on the line. The position of HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

HORIZONTAL AND VERTICAL SYNC WIDTH REGISTER (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allow the VL6845E to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

VERTICAL TOTAL REGISTER (R4)

This 7-bit register contains the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency RES may be used to provide absolute syncronism.

VERTICAL TOTAL ADJUST REGISTER (R5)

This 5-bit write-only register contains the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

VERTICAL DISPLAYED REGISTER (R6)

This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

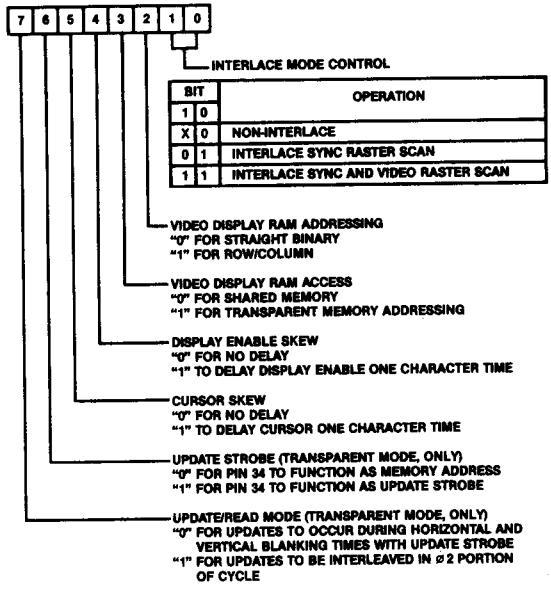
VERTICAL SYNC POSITION REGISTER (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

VL6845E REGISTER FILE DESCRIPTIONS (Cont.)

MODE CONTROL REGISTER (R8)

This register is used to select the operating modes of the VL6845E and is outlined as follows:



SCAN LINE REGISTER (R9)

This 5-bit register contains the number of scan lines per character row, including space minus one.

CURSOR START REGISTER (R10) AND CURSOR END REGISTER (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		
66	55	Cursor Display Mode
60	50	Non-Blink
60	51	Non-Display
61	50	Blink 1/16 Field Rate
61	51	Blink 1/32 Field Rate

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accomodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

DISPLAY START ADDRESS AND LOW REGISTERS (R12,R13)

These registers together comprise a 14-bit register whose contents are the memory address of the first character of the displayed scan (the character on the top left of the video display). Subsequent memory addresses are generated by the VL68465E as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well as via R12 and R13.

CURSOR POSITION HIGH AND LOW REGISTERS (R14,R15)

These registers together comprise a 14-bit register whose contents are the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, the Cursor output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the Cursor output by a full CCLK time to accomodate slow-access memories.

LPSTB HIGH AND LOW REGISTERS (R16,R17)

These registers together comprise a 14-bit register whose contents are the light pen strobe position, in terms of the video display address at which the strobe occured. When the LPSTB input changes from LOW to HIGH, then, on the next negative-going edge of CCLK, the contents of the internal scan counter are stored in registers R16 and R17.

UPDATE ADDRESS HIGH AND LOW REGISTERS (R18,R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent addressing mode, only). Whenever a read/update occurs, the update location automatically updates, to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

DUMMY LOCATION (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the Status Register.

VL6845E DESCRIPTION OF OPERATION

REGISTER FORMATS

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1) Straight Binary if register R8, bit2 is a zero.
2) Row/Column if register R8, bit 2 is a one. In this case, the low byte is the Character Column, and the high byte is the Character Row.

Figure 2 illustrates the address sequence for the video display control for each mode. Note from Figure 2 that the straight binary mode has the advantage that all display memory addresses

VL6845E
DESCRIPTION OF OPERATION
(Cont.)

are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not require this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous (gaps exist). This requires that the system be equipped with more memory than is actually used, and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the system designer may select whichever mode is best for the given application. The trade-offs between the modes involve the comparative costs of hardware and software. Straight-binary mode minimizes hardware requirements, and row/column addressing requires minimum software.

VIDEO DISPLAY RAM ADDRESS LINES (MA0-MA13)

These signals are active-HIGH outputs that are used to address the video display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters per line and lines per frame.

There are two selectable address modes for MA0-MA13:

1. Binary
   Characters are stored in successive memory locations. Thus, the software must be developed so that row and column coordinates are translated in sequentially numbered addresses for video display memory operations.
2. Row/Column
   In this mode, MA0-MA7 function as column addresses CC0-CC7, and MA8-MA13 as row addresses CR0-CR5. In this case, the software may handle addresses in terms of row and column locations, but additional address compression circuits are needed to convert CC0-CC7 and CR0-CR5 into a memory efficient binary scheme.

RASTER ADDRESS LINES (RA0-RA4)

These signals are active-HIGH outputs that are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The HIGH-order line, RA4, is unique in that it can also function as a strobe output pin when the VL6845E is programmed to operate in the "transparent address mode". In this case, the strobe is an active-HIGH output that is true at the time the video display RAM update address is gated onto the address lines, MA0-MA13. In this way, updates and readouts of the video display RAM can be made under control of the CRTC with only a small amount of external circuitry.

FIGURE 2. DISPLAY ADDRESS SEQUENCES (WITH START ADDRESS = 0) FOR 80 x 24 EXAMPLE

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	- - -	- - -	77	78	79	80	81	- - -	89
80	81	82	- - -	- - -	157	158	159	160	161	- - -	169
160	161	162	- - -	- - -	237	238	239	240	241	- - -	249
⋮							⋮				⋮
1760	1761	1762	- - -	- - -	1837	1838	1839	1840	1841	- - -	1849
1840	1841	1842	- - -	- - -	1917	1918	1919	1920	1921	- - -	1929
1920	1921	1922	- - -	- - -	1997	1998	1999	2000	2001	- - -	2009
2000	2001	2002	- - -	- - -	2077	2078	2079	2080	2081	- - -	2089
⋮							⋮				⋮
2640	2641	2642	- - -	- - -	2717	2718	2719	2720	2721	- - -	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

TOTAL = 90

DISPLAY = 80

COLUMN ADDRESS (MA0-MA7)

TOTAL = 34

DISPLAY = 24

ROW ADDRESS (MA8-MA13)

	0	1	2			77	78	79	80	81		89
0	0	1	2	- - -	- - -	77	78	79	80	81	- - -	89
1	256	257	258	- - -	- - -	333	334	335	336	337	- - -	345
2	512	513	514	- - -	- - -	589	590	591	592	593	- - -	601
⋮								⋮				⋮
21												
22	5632	5633	5634	- - -	- - -	5709	5710	5711	5712	5713	- - -	5721
23	5888	5889	5890	- - -	- - -	5965	5966	5967	5968	5969	- - -	5977
24	6144	6145	6146	- - -	- - -	6221	6222	6223	6224	6225	- - -	6233
25	6400	6401	6402	- - -	- - -	6477	6478	6479	6480	6481	- - -	6489
⋮								⋮				⋮
33	8448	8449	8450	- - -	- - -	8525	8526	8527	8528	8529	- - -	8537

ROW/COLUMN ADDRESSING SEQUENCE

VL6845E DESCRIPTION OF OPERATION (Cont.)

MEMORY CONTENTION SCHEMES FOR SHARED MEMORY ADDRESSING

In a typical system, it is clear that both the VL6845E CRTC and the system MPU must be capable of addressing the video display memory. The VL6845E CRTC repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

1. **MPU PRIORITY**
   In this technique, the address lines to the video display memory are normally driven by the VL6845E unless the MPU needs access, in which case the MPU addresses immediately override those from the VL6845E and the MPU has immediate access.
2. **PHASE 1/PHASE 2 (01/02) MEMORY INTERLEAVING**
   This method permits both the VL6845 and the MPU access the video display memory by time-sharing via system 01 and 02 clocks. During the 01 portion of each cycle (the time when E is LOW), the CRTC address outputs are gated to the video display memory. In the 02 time, the MPU address lines are switched in. In this way, both the CRTC and the MPU have unimpeded access to the memory. (Figure 3a illustrates the timings)
3. **VERTICAL BLANKING**
   With this approach, the address Circuitry is identical to the case for MPU priority updates. The only difference is that the vertical retrace status bit (bit 5 of the status register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a one). In this way, no visible screen perturbations result.

TRANSPARENT MEMORY ADDRESSING

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the CRTC. In effect, the contention is handled by the CRTC. As a result, the schemes for accomplishing MPU memory acces are different:

1. **PHASE 1/PHASE 2 (Ø1/Ø2) INTERLEAVING**
   This mode is similar to the interleave mode used with shared memory. In this case, however, the Ø2 address is generated from the update address register (Registers R18 and R19) in the CRTC. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during Ø2. (Figure 3b illustrates the timing)
2. **HORIZONTAL/VERTICAL BLANKING**
   In this mode, the update address register is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternative function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted while waiting for the blanking time to arrive.

FIGURE 3a. PHASE 1/PHASE 2 SHARED INTERLEAVING

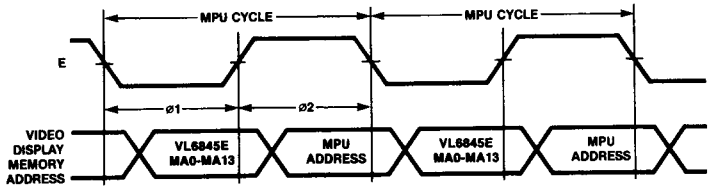
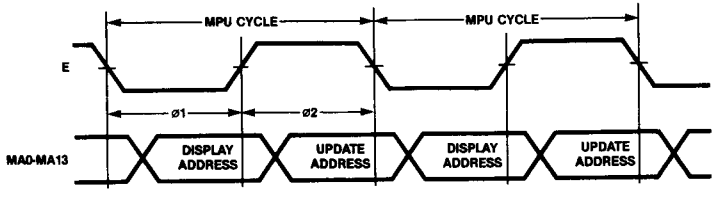


FIGURE 3b. PHASE 1/PHASE 2 TRANSPARENT INTERLEAVING



ABSOLUTE MAXIMUM RATINGS

Supply Voltage −0.3 V to +7.0 V

Input/Output Voltage, VIN −0.3 V to +7.0 V

Operating Temperature, Top 0°C to 70°C

Storage Temperature, TSTG −55°C to 150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0° to 70°C, VCC = 5.0 V ± 5%, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit
VIH	Input HIGH Voltage	2.0		Vcc	V
VIL	Input LOW Voltage	−0.3		0.8	V
IIN	Input Leakage (o2, R/W, RES, CS, RS, LPSTB, CCLK)	—		2.5	μA
ITSI	Three-State Input Leakage (DBO-DB7) VIN = 0.4 to 2.4 V	—		±10.0	μA
VOH	Output HIGH Voltage ILOAD = −205 μA (DBO-DB7) ILOAD = −100 μA (all others)	2.4		—	V
VOL	Output LOW Voltage ILOAD = 1.6 mA	—		0.4	V
PD	Power Dissipation	—	325	650	mW
CI	Input Capacitance o2,R/W,RES,CS,RS,LPSTB,CLK, DBO-DB7	— —		10.0 12.5	pF pF
CO	Output Capacitance	—		10.0	pF

VL6845 CHARACTERISTICS

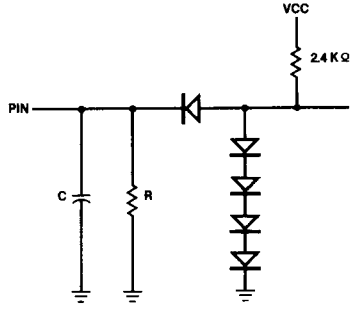
To ensure system compatibility, all CRTC timing is referenced by bus and character clock speed specification rather than device type. Thus, for a given MPU and character clock speed, the entire VL6845 family will adhere to the same timing regardless of version number. Table 13 presents a cross reference between specifications and device numbers.

The bus timing test load is shown in Figure 4. Signal timing for the CRTC is described in Table 14, and Table 15 describes CRTC video timing. Light pen timing is described in Table 16.

TABLE 13: VL6845 SPECIFICATION/ PART NUMBER REFERENCE

VL6845E-24	VTI-24
VL6845E-34	VTI-34
VL6845R-23	VTI-23
VL6845R-24	VTI-24
VL6845R-33	VTI-33
VL6845R-34	VTI-34
VL6845R-35	VTI-35
VL68C45R-23	VTI-23
VL68C45R-24	VTI-24
VL68C45R-33	VTI-33
VL68C45R-34	VTI-34
VL68C45R-35	VTI-35
VL68C45S-23	VTI-23
VL68C45S-24	VTI-24
VL68C45S-33	VTI-33
VL68C45S-34	VTI-34
VL68C45S-35	VTI-35

FIGURE 4. TEST LOAD



R = 11 KΩ FOR DB0—DB7
R = 24 KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR DO—D7
C = 30 pF ALL OTHER OUTPUTS

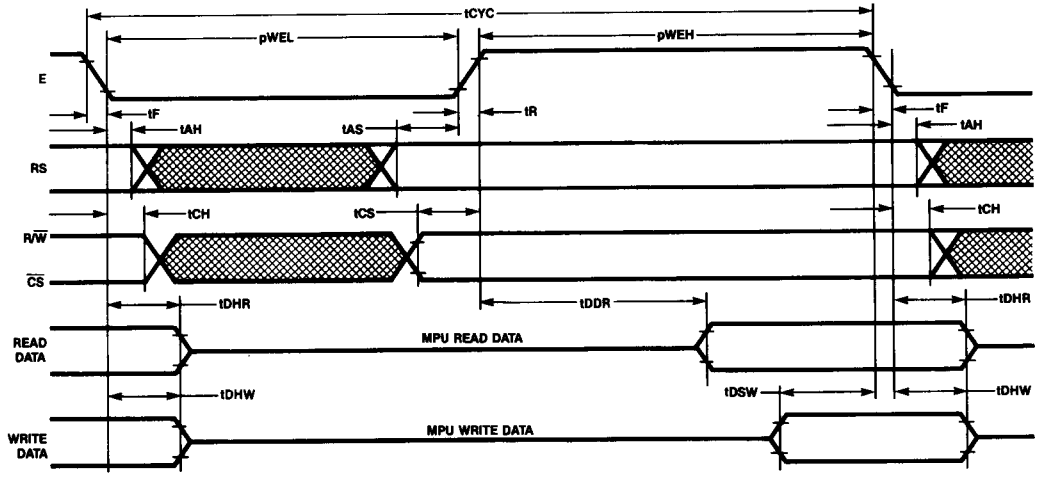
NOTES:
1. VOLTAGE LEVELS SHOWN ARE 0.4 V AND 2.4 V
2. MEASUREMENT POINTS SHOWN ARE 0.8 V AND 2.0 V

VL6845
CHARACTERISTICS (Cont.)
TABLE 14: CRTC BUS TIMING CHARACTERISTICS

Symbol	Parameter	VTI-23		VTI-24		VTI-33		VTI-34 VTI-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
tcyc	Cycle Time	500		500		333		333		ns
pWEL	Pulse Width, E LOW	190		190		140		140		ns
pWEH	Pulse Width, E HIGH	200		200		150		150		ns
tR	Clock Rise Time		30		30		30		30	ns
tF	Clock Fall Time		30		30		30		30	ns
tAH	Address Hold Time (RS)	0		0		0		0		ns
tAS	RS Setup Time	40		40		30		30		ns
tCS	R/W, CS Setup	40		40		30		30		ns
tCH	R/W, CS Hold Time	0		0		0		0		ns
tDHR	Read Data Hold Time	20	60	20	60	20	60	20	60	ns
tDHW	Write Data Hold Time	10		10		10		10		ns
tDDR	Peripheral Output Delay Time	0	150	0	150	0	130	0	130	ns
tDSW	Peripheral Setup Time	60		60		60		60		ns

TIMING DIAGRAM

VL6845 BUS TIMING



NOTES:
1. VOLTAGE LEVELS SHOWN ARE V1≤ 0.4V, Vh≥ 2.4V
2. MEASUREMENT POINTS SHOWN ARE 0.8V AND 2.0V.

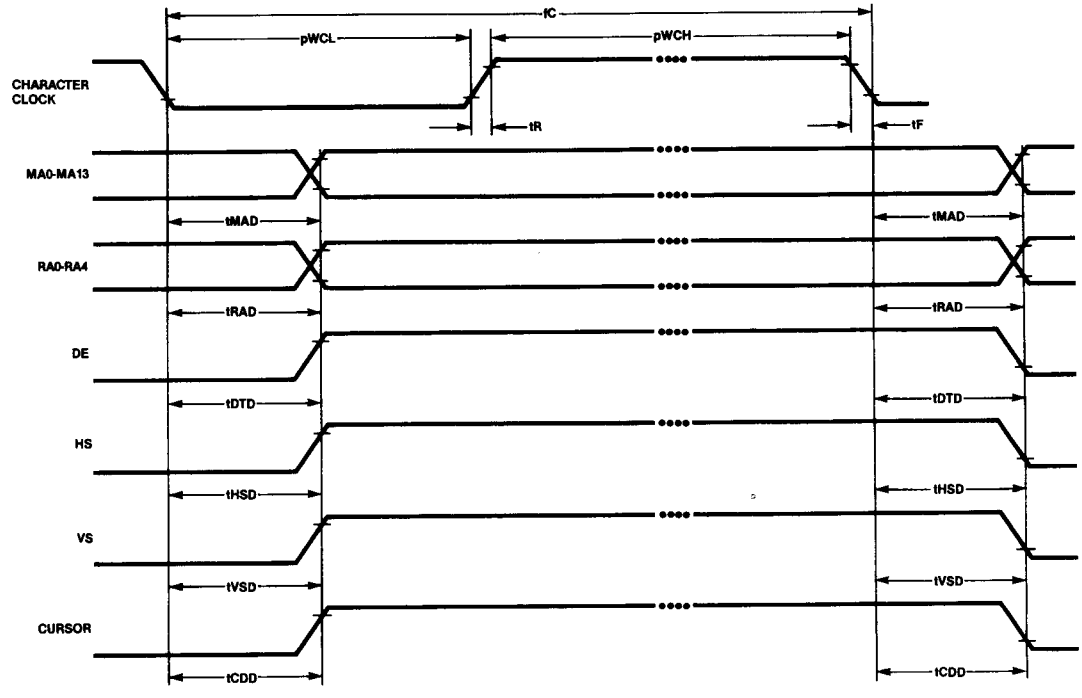
VL6845
CHARACTERISTICS (Cont.)

TABLE 15: CRTC VIDEO TIMING CHARACTERISTICS

Symbol	Parameter	VTI-23		VTI-24		VTI-33		VTI-34		VTI-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
pWCL	Clock Pulse Width, LOW	150		110		150		110		100		ns
pWCH	Clock Pulse Width, HIGH	150		120		150		120		100		ns
fC	Clock Frequency		3.0		4.0		3.0		4.0		5.0	MHz
tR	Clock Rise Time		20		20		20		20		20	ns
tF	Clock Fall Time		20		20		20		20		20	ns
tMAD	Memory Address Delay Time		160		140		160		140		140	ns
tRAD	Raster Address Delay Time		160		150		160		150		140	ns
tDTD	Display Timing Delay Time		250		250		250		250		200	ns
tHSD	Horizontal Sync Delay Time		250		200		250		200		200	ns
tVSD	Vertical Sync Delay Time		250		250		250		250		200	ns
tCDD	Cursor Display Delay Time		250		250		250		250		200	ns

TIMING DIAGRAM

VL6845 VIDEO TIMING



NOTES:
TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE SPECIFIED

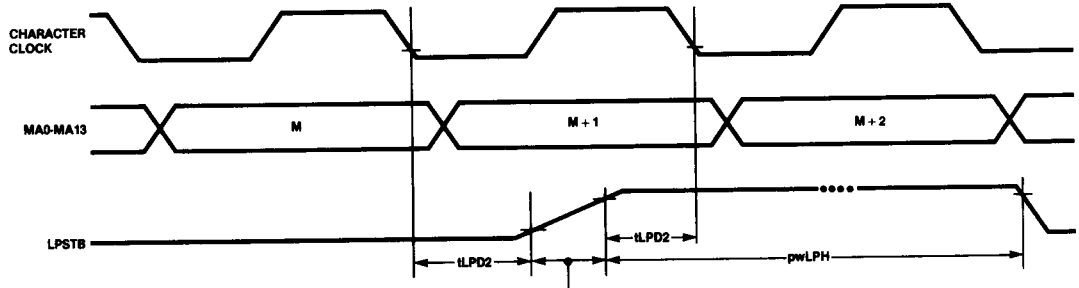
VL6845
AC CHARACTERISTICS

TABLE 16: CRTC LIGHT PEN TIMING CHARACTERISTICS

Symbol	Parameter	VTI-23		VTI-24		VTI-33		VTI-34 VTI-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
pwLPH	Light Pen Strobe Pulse Width	80		60		80		60		ns
tLPD1	Light Pen Display Time 1		120		70		120		70	ns
tLPD2	Light Pen Display Time 2		0		0		0		0	ns

TIMING DIAGRAM

VL6845 LIGHT PEN TIMING



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. tLPD1 AND tLPD2 ARE THE PERIODS OF UNCERTAINTY FOR THE REFRESH MEMORY ADDRESS.

CROSS REFERENCE GUIDE

VTI Device	Replaces	Bus Frequency (MHz)	Character Clock (MHz)
VL6845R-23	MC68B45R	2.0	3.0
VL6845R-23	MC68A45	1.5	3.0
VL6845R-23	MC6845R	1.0	3.0
VL68C45R-23	MC68B45R1	2.0	3.0
VL68C45R-23	MC68A45R1	1.5	3.0
VL68C45R-23	MC6845R1	1.0	3.0
VL68C45R-23	HD68B45R	2.0	3.0
VL68C45R-23	HD68A45R	1.5	3.0
VL68C45R-23	HD6845R	1.5	3.0
VL68C45S-24	HD68B45S	2.0	3.7
VL68C45S-24	HD68A45S	1.5	3.7
VL68C45S-24	HD6845S	1.0	3.7
VL6845E-24	SY6845EA	2.0	3.7
VL6845E-24	SY6845E	1.0	3.7
VL6845R-23	SY6845RA	2.0	2.5
VL6845R-23	SY6845R	1.0	2.5

VL6845 REGISTER COMPARISON

Non-Interlace

Register	VL68C45R MC6845R1	VL6845R MC6845 HD6845R	VL68C45S HD6845S	SY6545-1	VL6845E
R0 Horizontal Tot	Tot-1	Tot-1	Tot-1	Tot-1	Tot-1
R1 Horizontal Disp	Actual	Actual	Actual	Actual	Actual
R2 Horizontal Sync	Actual	Actual	Actual	Actual	Actual
R3 Horizontal and Vert Sync Width	Horizontal	Horizontal	Horizontal and Vertical	Horizontal and Vertical	Horizontal and Vertical
R4 Vertical Tot	Tot-1 (0-127)	Tot-1	Tot-1	Tot-1	Tot-1
R5 Vertical Tot Adj	Any Value	Any Value	Any Value	Any Value Except R5 = (R9H) • X	Any Value
R6 Vertical Disp	Any Value <R4 (0-255)	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vertical Sync Pos	Actual-1 (0-255)	Actual-1	Actual-1	Actual-1	Actual-1
R8 Mode Reg Bits 0 and 1	Interlace Mode Select	Interlace Mode Select	Interlace Mode Select	Interlace Mode Select	Interlace Mode Select
Bits 2	—	—	—	Row/Column or Straight Binary Addressing	Row/Column or Straight Binary Addressing
Bits 3	—	—	—	Shared or Transparent Addr	Shared or Transparent Addr
Bits 4	—	—	Dispen Skew	Dispen Skew	Dispen Skew
Bits 5	—	—	Dispen Skew	Cursor Skew	Cursor Skew
Bits 6	—	—	Cursor Skew	RA4/UPSTB	RA4/UPSTB
Bits 7	—	—	Cursor Skew	Transparent Mode Select	Transparent Mode Select
R9 Scan Lines	Tot-1	Tot-1	Tot-1	Tot-1	Tot-1
R10 Cursor Start	Actual	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual	Actual
R12/R13 Disp Addr	Write Only	Write Only	Read/Write	Write Only	Write Only
R14/R15 Cursor POS	Write Only	Write Only	Read/Write	Read/Write	Read/Write
R16/R17 Lpen Reg	Read Only	Read Only	Read Only	Read Only	Read Only
R18/R19 Update Addr Reg	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
R31 Dummy Reg	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
Status Reg	No	No	No	Yes	Yes
Interlace Sync					
R0	Tot-1 = Odd	Tot-1 = Odd	Tot-1 = Odd	Tot-1 = Odd	Tot-1 = Odd or Even
Interlace Sync and Video					
R4 Vertical	Tot-1	Tot-1	Tot-1	Tot/2-1	Tot-1
R6 Vert Disp	Tot/2	Tot/2	Tot	Tot/2	Tot
R7 Vert Sync	Actual-1	Actual-1	Actual-1	Actual/2	Actual-1
R9 Scan Lines	Tot-2 Odd/Even	Tot-1 Only Even	Tot-2 Odd/Even	Tot-1 Odd/Even	Tot-1 Odd/Even
R10 Cursor Start R11 Cursor End	Both Odd or Both Even	Both Odd or Both Even	Odd/Even Odd/Even	Odd/Even Odd/Even	Odd/Even Odd/Even

VMC68C45 MEGACELL DESIGN KIT
CRT CONTROLLER MEGACELL

FEATURES

- Completely integrated with VTI's extensive IC design tools and libraries
- 2-micron CMOS 68C45 Megacell configurable as:
  - 68C45R — CMOS equivalent to Motorola 6845R CRTC
  - 68C45R1 — CMOS equivalent to Motorola 6845R1 Enhanced CRTC
  - 68C45S — CMOS equivalent to Hitachi 6845S CRTC
  - 68C45SY — CMOS CRTC similar to Synertek 6545 CRTC
- 4.5 MHz video memory interface
- 3 MHz system processor interface
- Compatible with the VTI bus architecture
- Programmable Display Enable and Cursor delays (standard for S and SY versions—optional for R version)
- Row/column display memory addressing (SY version)
- Double-width character control

OPTIONAL FEATURES

- 16K, 32K, or 64K display Memory Address range (14-, 15-, or 16-bits)
- Programmable Vertical Sync pulse width
- 7-, 8-, or 9-bit Vertical Row counter

DESCRIPTION

Megacells are building block equivalents of standard LSI functions that can be combined with other megacells, standard cells or compiled cells to create custom User Specific ICs (USICs). Megacells are fully compatible with VTI's other cell technologies and design tools.

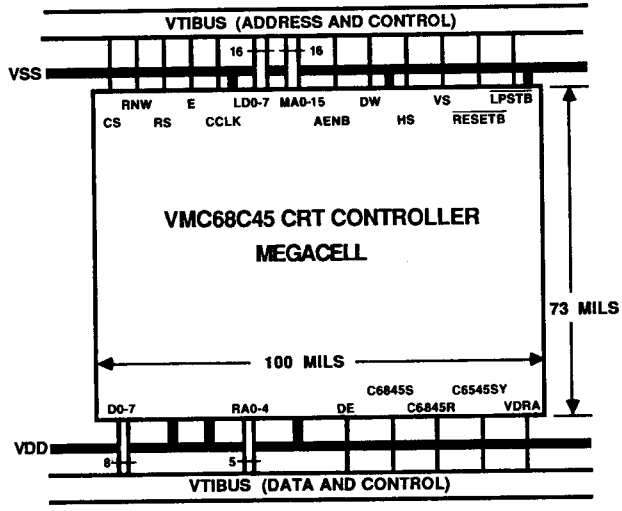
The VTI bus architecture allows multiple megacells to be combined on a single IC, along with additional cells from VTI's extensive libraries. This decreases the design time, cost and size of complex systems. A detailed simulation model provided with each megacell further reduces design verification time.

VMC68C45 MEGACELL DESIGN KIT DESCRIPTION

The VMC68C45 Megacell Design Kit includes the simulation models and icons required to permit designers using VTI's IC design tools to develop custom CRT controller designs.

Using the proven 68C45 LSI functional building block, implementing a specific CRT controller application requires only the combination of a 68C45 megacell with other logic on one or more VLSI ICs. For example, if a 68C45 megacell is combined with a ROM megacell character generator and "glue" logic, a complete CRT adapter for monochrome or color applications can be designed.

CONNECTOR DIAGRAM



SIGNAL DESCRIPTIONS

The following signals function the same on the VMC68C45 megacells and on the VL6845 family of CRT Controller ICs.

Signal	I/O	Description
RS	Input	Register Select
E	Input	Enable
CCLK	Input	Character Clock
LPSTB	Input	Light Pen Strobe
D0-D7	Input/Output	Data Bus
RA0-RA4	Output	Raster Address
HS	Output	Horizontal Sync
RESETB	Output	Reset

The following signals are unique or enhanced on the VMC68C45 megacells.

Signal	I/O	Description
RNW	Input	Same as R/$\overline{W}$, input on VL6845.
CS	Input	Same input as on VL6845, except active HIGH.
DW	Input	Double-width input—this input places the 68C45 in a double-width display mode.
AENB	Input	Address Enable input—when asserted LOW (AENB = "0") the MA outputs are enabled. AENB = "1" forces the MA outputs into a HIGH impedance state.
C6845R, C6845S, C6545SY	Input	One of these three inputs is tied HIGH to select the version of the 68C45 used in your application. The remaining two inputs must be grounded. NOTE: the 68C45SY megacell does not provide 6545 transparent addressing or the 6545 status register.
MA0-MA13, 14, 15	Output	14-, 15-, or 16-bit Video Memory Address bus—These tri-state outputs provide the binary address to the external video RAM. If row/column addressing is selected (SY version only) this bus will provide row/column addressing to the external RAM instead of binary addressing. The AENB input signal can be used to place the MA bus in the HIGH impedance state.
DE	Output	Display Enable output—active (DE = "1") when the 68C45 is generating active display information. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
CURSOR	Output	Cursor output—this signal is HIGH when the raster scan coincides with the programmed cursor position. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
VS	Output	Vertical Sync output—active HIGH pulse which determines the vertical placement of the video data. An optional feature permits programming the Vertical Sync pulse width.
LD0-LD13, 14, 15	Input/ Output	14-, 15-, or 16-bit Advanced Memory Address bus—separate video memory address information on this bus precedes the information on the MA bus by one character clock. This bus is provided to interface with a separate strip of logic for split display capability.
VDRA (reserved)	n/c	Reserved for future expansion—to be left unconnected.

ORDER INFORMATION

VMC68C45-c*-m** Complete Design Kit for CMOS 68C45 Megacell

*c	Computer Type
A	Apollo workstation
V	VAX workstation
R	RIDGE workstation
E	ELXSI workstation
W	WANG workstation

**m	Media Format
1	Floppy diskette
2	Magnetic tape
3	Cartridge