MOTOROLA

Advance Information

ROM—I/O—TIMER

The MC6846 combination chip provides the means, in conjunction with the MC6802, to develop a basic 2-chip microcomputer system. The MC6846 consists of 2048 bytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable timer-counter.

This device is capable of interfacing with the MC6802 (basic MC6800, clock and 128 bytes of RAM) as well as the MC6800 if desired. No external logic is required to interface with most peripheral devices.

- 2048 8-Bit Bytes of Mask-Programmable ROM
- 8-Bit Bidirectional Data Port for Parallel Interface plus Two Control Lines
- Programmable Interval Timer-Counter Functions
- Programmable I/O Peripheral Data, Control and Direction Registers
- Compatible with the Complete M6800 Microcomputer Product Family
- TTL-Compatible Data and Peripheral Lines
- Single 5-Volt Power Supply

MOS

(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

ROM—I/O—TIMER
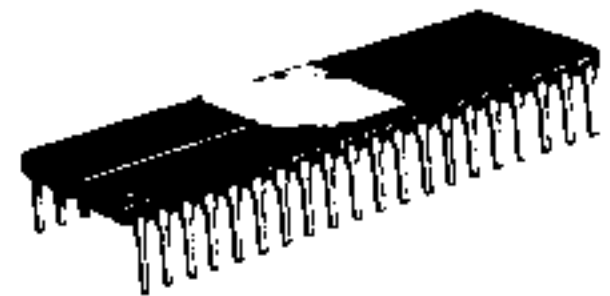
L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN:
P SUFFIX
PLASTIC PACKAGE
CASE 711

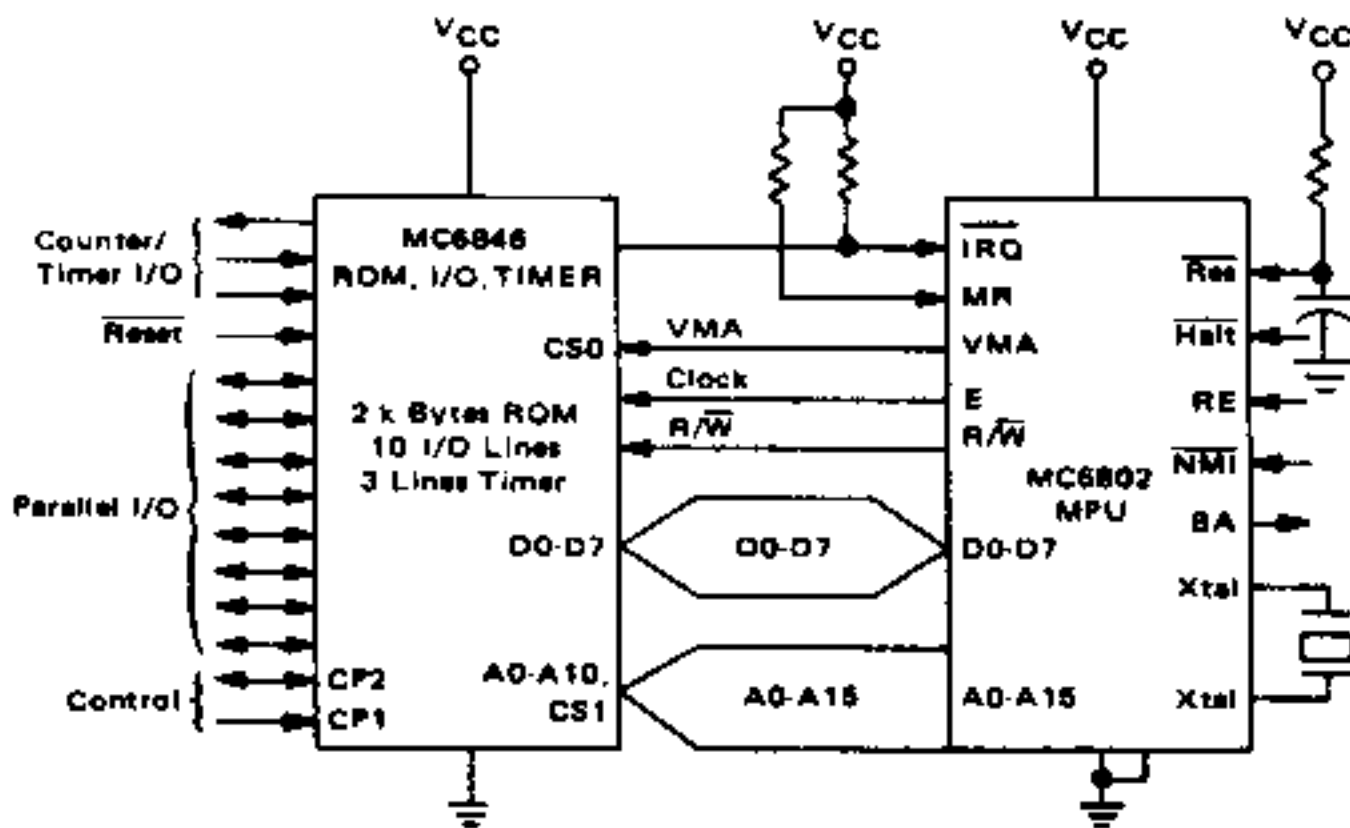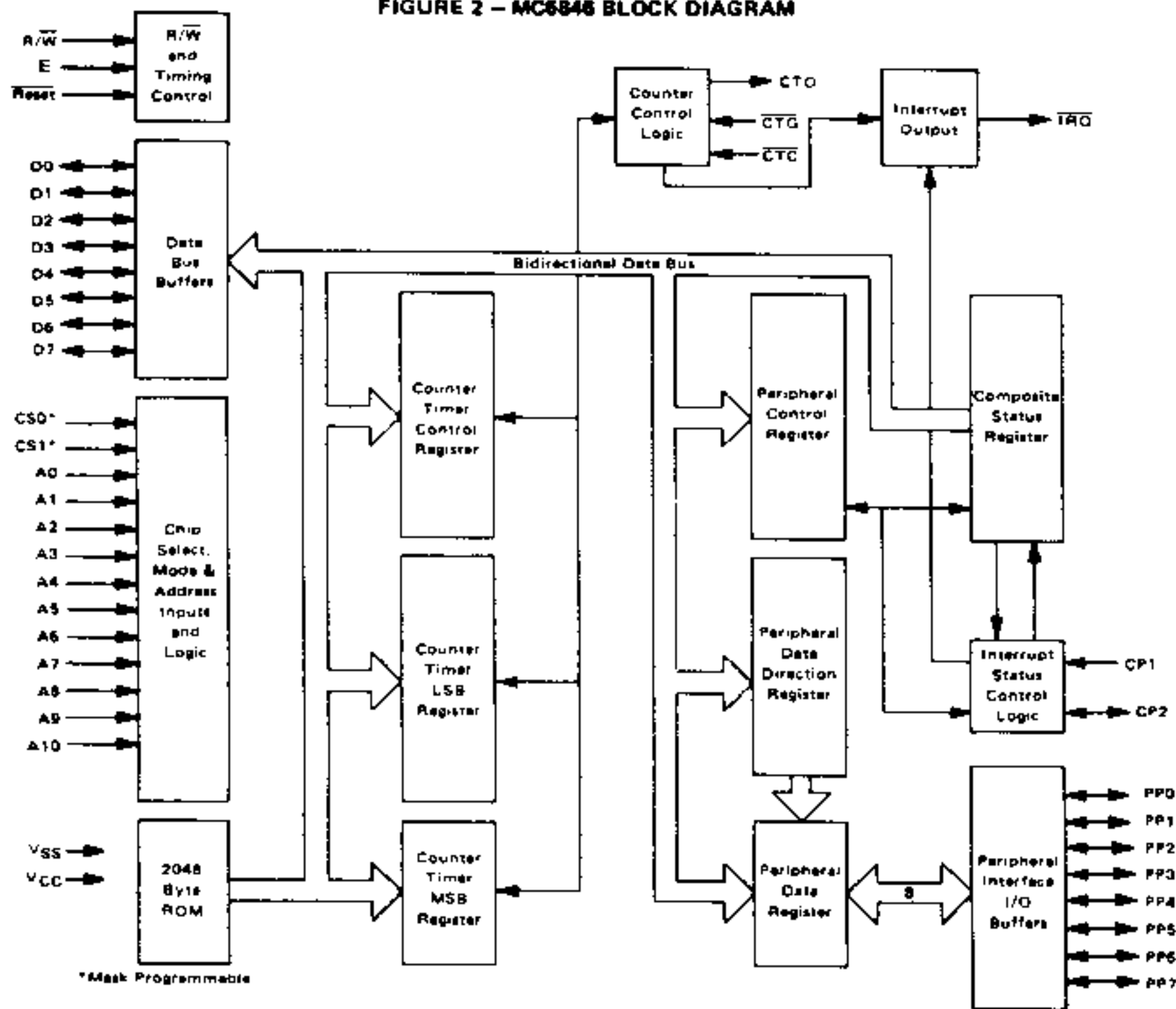### FIGURE 1 — TYPICAL MICROCOMPUTER

Figure 1 is a block diagram of a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the M6800 Microcomputer family.

ROM — I/O — TIMER

1	V$_{SS}$	A8 — 40
2	A7	A9 — 39
3	A6	A10 — 38
4	A5	RES — 37
5	A4	IRQ — 36
6	CS0	CP2 — 35
7	R/W	CP1 — 34
8	D0	A0 — 33
9	D1	A1 — 32
10	D2	A2 — 31
11	D3	A3 — 30
12	D4	V$_{CC}$ — 29
13	D5	P7 — 28
14	D6	P6 — 27
15	D7	P5 — 26
16	CS1	P4 — 25
17	CTG	P3 — 24
18	CTC	P2 — 23
19	CTO	P1 — 22
20	E	P0 — 21

This is advance information and specifications are subject to change without notice.

MC6846

FIGURE 2 — MC6846 BLOCK DIAGRAM

FIGURE 2 — MC6846 BLOCK DIAGRAM

*Mask Programmable

GENERAL DESCRIPTION

The MC6846 combination chip may be partitioned into three functional operating sections: programmed storage, timer-counter functions, and a parallel I/O port.

Programmed Storage

The mask-programmable ROM section is similar to other ROM products of the M6800 family. The ROM is organized in a 2048 by 8-bit array to provide read only storage for a minimum microcomputer system. Two mask-programmable chip selects are available for user definition.

Address inputs A0–A10 allow any of the 2048 bytes of ROM to be uniquely addressed. Bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the MC6846.

Timer-Counter Functions

Under software control this 16-bit binary counter may be programmed to count events, measure frequencies, time intervals, or similar tasks. Internal registers associated with the I/O functions may be selected with A0, A1 and A2. It may also be used for square wave generation, single pulses of controlled duration, and gated signals. Interrupts may be generated from a number of conditions selectable by software programming.

The timer/counter control register allows control of the interrupt enable, output enable, selection of an internal or external clock source, a ÷ 8 prescaler, and operating mode. Input pin $\overline{CTC}$ (counter-timer clock) will accept an asynchronous clock pulse to decrement the internal register for the counter-timer. If the divide-by-8 prescaler is used, the maximum clock rate can be four times the master clock frequency with an absolute maximum of 4 MHz. Gate input ($\overline{CTG}$) accepts an asynchronous TTL-compatible signal which may be used as a trigger or gating function to the counter-timer. A counter-timer output (CTO) is also available and is under software control being dependent on the timer control register, the gate input, and the clock source.

Parallel I/O Port

The parallel bidirectional I/O port has functional operational characteristics similar to the B port on the MC6820 PIA. This includes 8 bidirectional data lines and two handshake control signals. The control and operation of these lines are completely software programmable.

The interrupt input (CP1) will set the interrupt flag CSR1 of the composite status register. The peripheral control (CP2) may be programmed to act as an interrupt input (set CSR2) or as a peripheral control output.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	70	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, is is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS $(V_{CC} = 5.0 \text{ V} \pm 5\%, V_{SS} = 0, T_A = 0 \text{ to } 70°C \text{ unless otherwise noted.})$

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	All Inputs	V_{IH}	$V_{SS} + 2.0$	−	V_{CC}	Vdc
Input Low Voltage	All Inputs	V_{IL}	$V_{SS} - 0.3$	−	$V_{SS} + 0.8$	Vdc
Clock Overshoot/Undershoot − Input High Level		V_{OS}	$V_{CC} - 0.5$	−	$V_{CC} + 0.5$	Vdc
− Input Low Level			$V_{SS} - 0.5$	−	$V_{SS} + 0.5$	
Input Leakage Current	R/W, Reset, CS0, CS1	I_{in}	−	1.0	2.5	μAdc
(V_{in} = 0 to 5.25 Vdc)	CP1, $\overline{CTG}$, $\overline{CTC}$, E, A0-A10					
Three-State (Off State) Input Current	D0-D7	I_{TSI}	−	2.0	10	μAdc
(V_{in} 0.4 to 2.4 Vdc)	PP0-PP7, CP2					
Output High Voltage		V_{OH}				Vdc
(I_{Load} = −205 μAdc,)	D0-D7		$V_{SS} + 2.4$	−	−	
(I_{Load} = −200 μAdc)	Other Outputs		$V_{SS} + 2.4$	−	−	
Output Low Voltage		V_{OL}				Vdc
(I_{Load} = 1.6 mAdc)	D0-D7		−	−	$V_{SS} + 0.4$	
(I_{Load} = 3.2 mAdc)	Other Outputs		−	−	$V_{SS} + 0.4$	
Output High Current (Sourcing)		I_{OH}				μAdc
(V_{OH} = 2.4 Vdc)	D0-D7		−205	−	−	
	Other Outputs		−200	−	−	
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g.,						
Darlington Base)	CP2, PP0-PP7		−1.0	−	−10	mAdc
Output Low Current (Sinking)		I_{OL}				mAdc
(V_{OL} = 0.4 Vdc)	D0-D7		1.6	−	−	
	Other Outputs		3.2	−	−	
Output Leakage Current (Off State)	$\overline{IRQ}$	I_{LOH}	−	−	10	μAdc
(V_{OH} = 2.4 Vdc)						
Power Dissipation		P_D	−	−	1000	mW
Capacitance		C_{in}	−	−	20	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7		−	−	12.5	
	PP0-PP7, CP2		−	−	10	
A0-A10, R/W, Reset, CS0, CS1, CP1, $\overline{CTC}$, $\overline{CTG}$			−	−	7.5	
	$\overline{IRQ}$					
	PP0-PP7, CP2, CT0	C_{out}		−	5.0	pF
				−	10	
Frequency of Operation		f	0.1	−	1.0	MHz
Clock Timing						
Cycle Time		t_{cycE}	1.0	−	−	μs
Reset Low Time		t_{RL}	2	−	−	μs
Interrupt Release		t_{IR}	−	−	1.6	μs

READ/WRITE TIMING (Figures 3 and 4).

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Pulse Width, Low	PW_{EL}	430	—	—	ns
Enable Pulse Width, High	PW_{EH}	430	—	—	ns
Set Up Time (Address CS0, CS1, R/W)	t_{AS}	160	—	—	ns
Data Delay Time	t_{DDR}	—	—	320	ns
Data Hold Time	t_H	10	—	—	ns
Address Hold Time	t_{AH}	10	—	—	ns
Rise and Fall Time	t_{Ef}, t_{Er}	—	—	25	ns
Data Set Up Time	t_{DSW}	195	—	—	ns

BUS TIMING
Peripheral I/O Lines

Characteristic	Symbol	Min	Typ	Max	Unit
Peripheral Data Setup	t_{PDSU}	200	—	—	ns
Rise and Fall Times CP1, CP2	t_{Pr}, t_{Pc}	—	—	1.0	μs
Delay Time E to CP2 Fall	t_{CP2}	—	—	1.0	μs
Delay Tme I/O Data CP2 Fall	t_{DC}	20	—	—	ns
Delay Time E to CP2 Rise	t_{RS1}	—	—	1.0	μs
Delay Time CP1 to CP2 Rise	t_{RS2}	—	—	2.0	μs
Peripheral Data Delay	t_{PDW}	—	—	1.0	μs
Peripheral Data Setup Time for Latch	t_{PSU}	100	—	—	ns
Peripheral Data Hold Time for Latch	t_{PDH}	15	—	—	ns

Timer Counter Lines

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Time	CTC and CTG	t_{CR}, t_{CF}	—	—	100	ns
Input Pulse Width High (Asynchronous Mode)		t_{PWH}	$t_{cyc} + 250$	—	—	ns
Input Pulse Width Low (Asychronous Mode)		t_{PWL}	$t_{cyc} + 250$	—	—	ns
Input Setup Time (Synchronous Mode)		t_{su}	200	—	—	ns
Input Hold Time (Synchronous Mode)		t_{hd}	50	—	—	ns
Output Delay		t_{CTO}	—	—	1.0	μs

FIGURE 3 — BUS READ TIMING
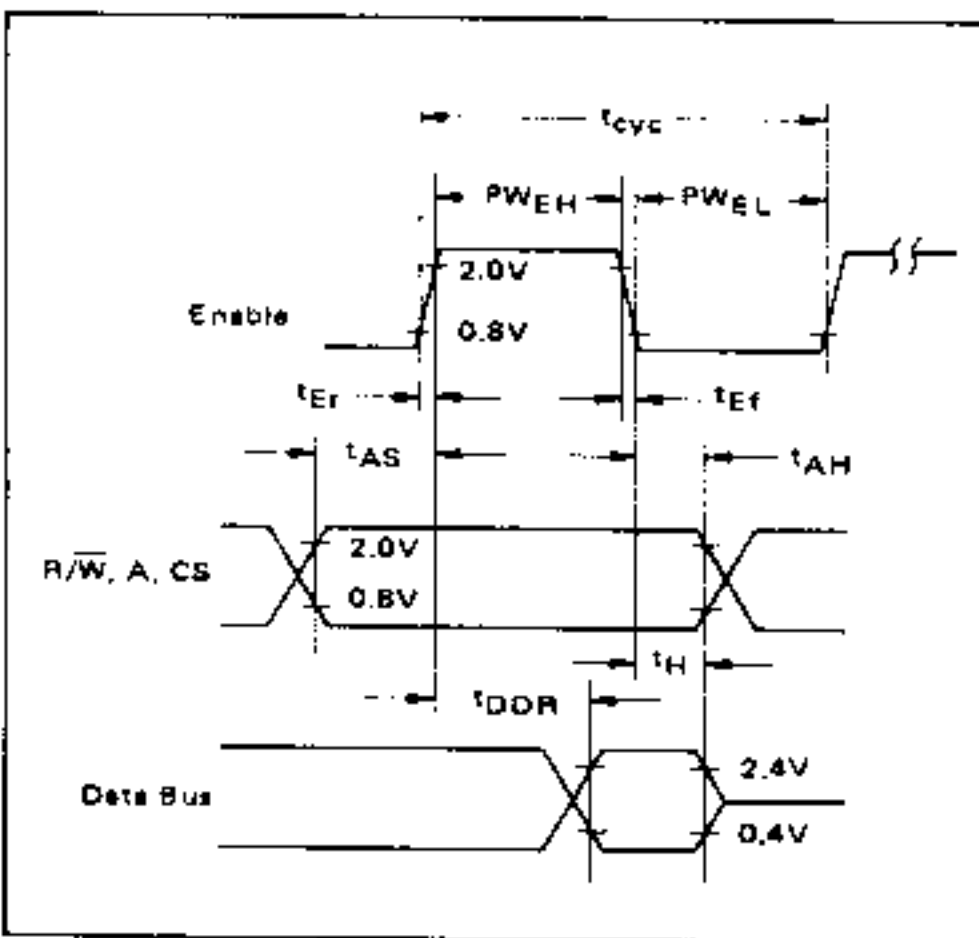Read Information from MC6846)

FIGURE 4 — BUS WRITE TIMING
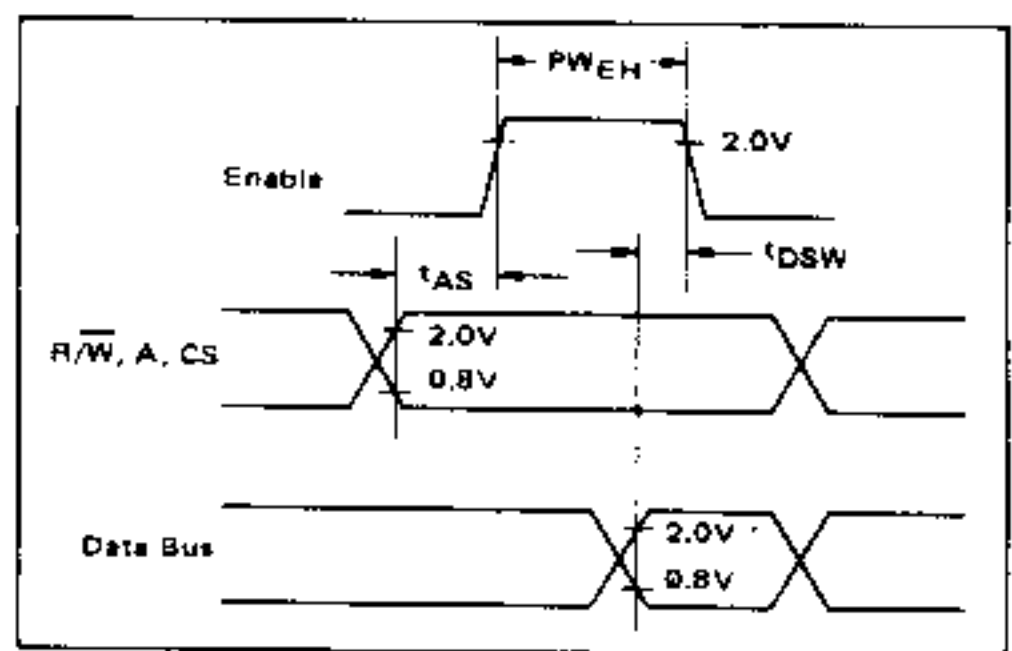(Write Information from MPU)
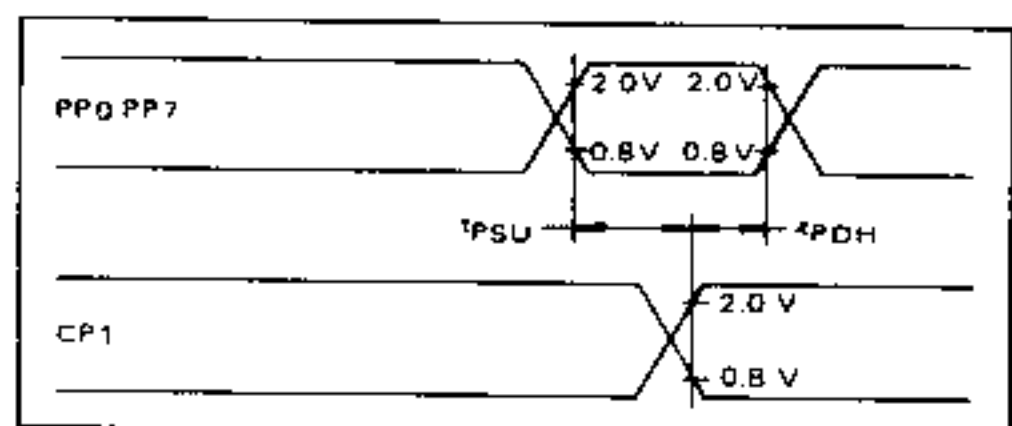

FIGURE 5 — PERIPHERAL PORT LATCH SETUP AND HOLD TIME

MC6846

FIGURE 6 — PERIPHERAL DATA AND CP2 DELAY
(Control Mode PCR5=1, PCR4=0, PCR3=1)

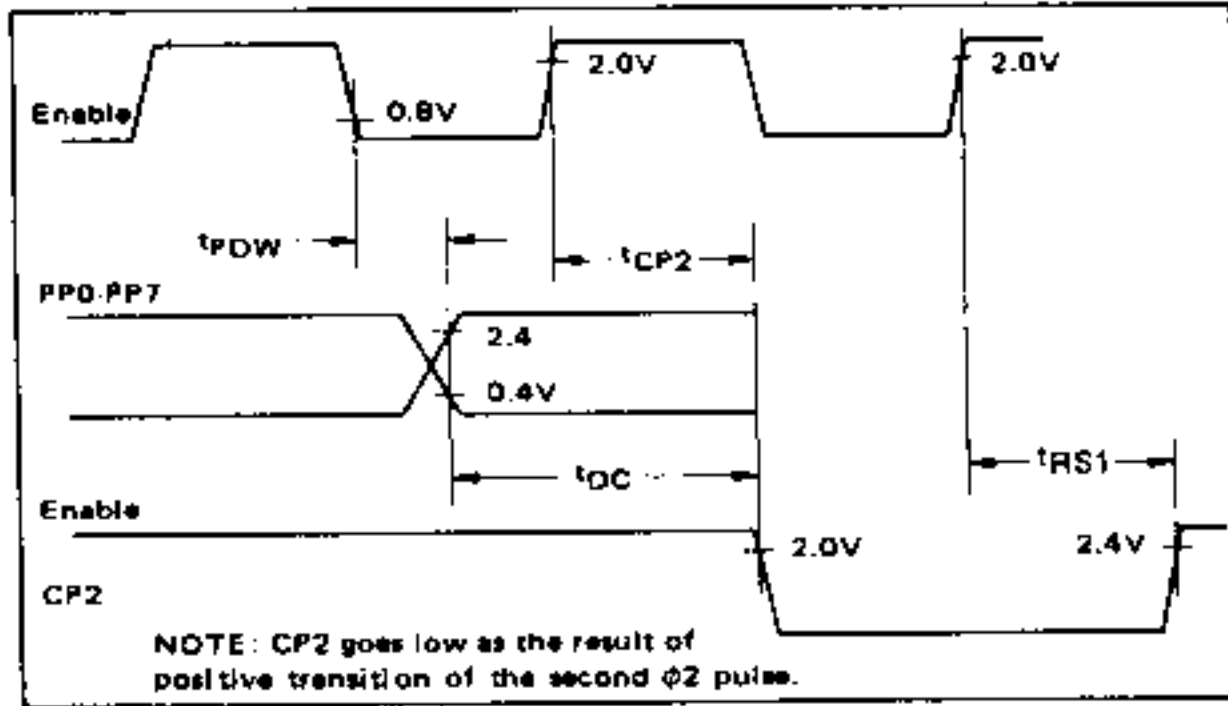NOTE: CP2 goes low as the result of positive transition of the second φ2 pulse.
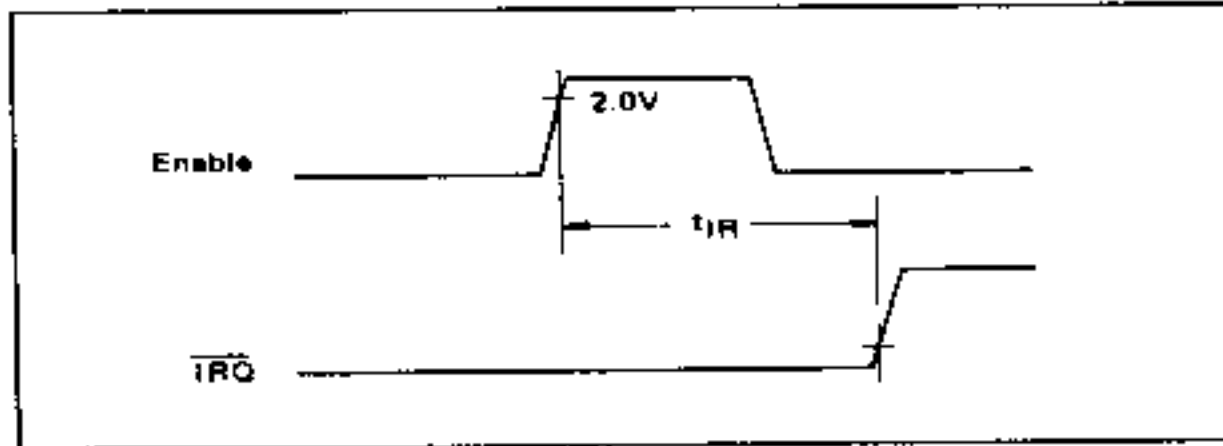
FIGURE 7 — IRQ RELEASE TIME

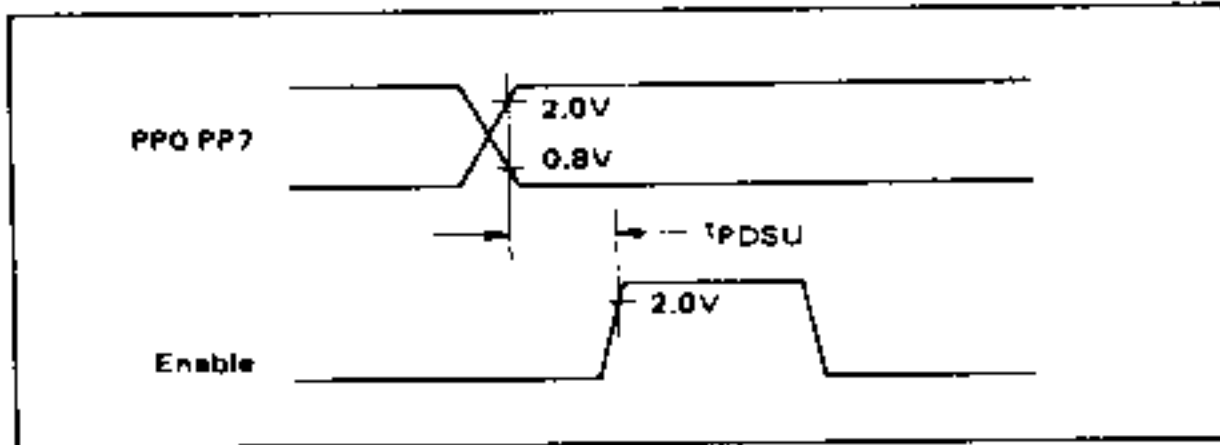## FIGURE 8 — PERIPHERAL PORT SETUP TIME

FIGURE 9 — CP2 DELAY TIME
(PCR5=1, PCR4=0, PCR3=0)
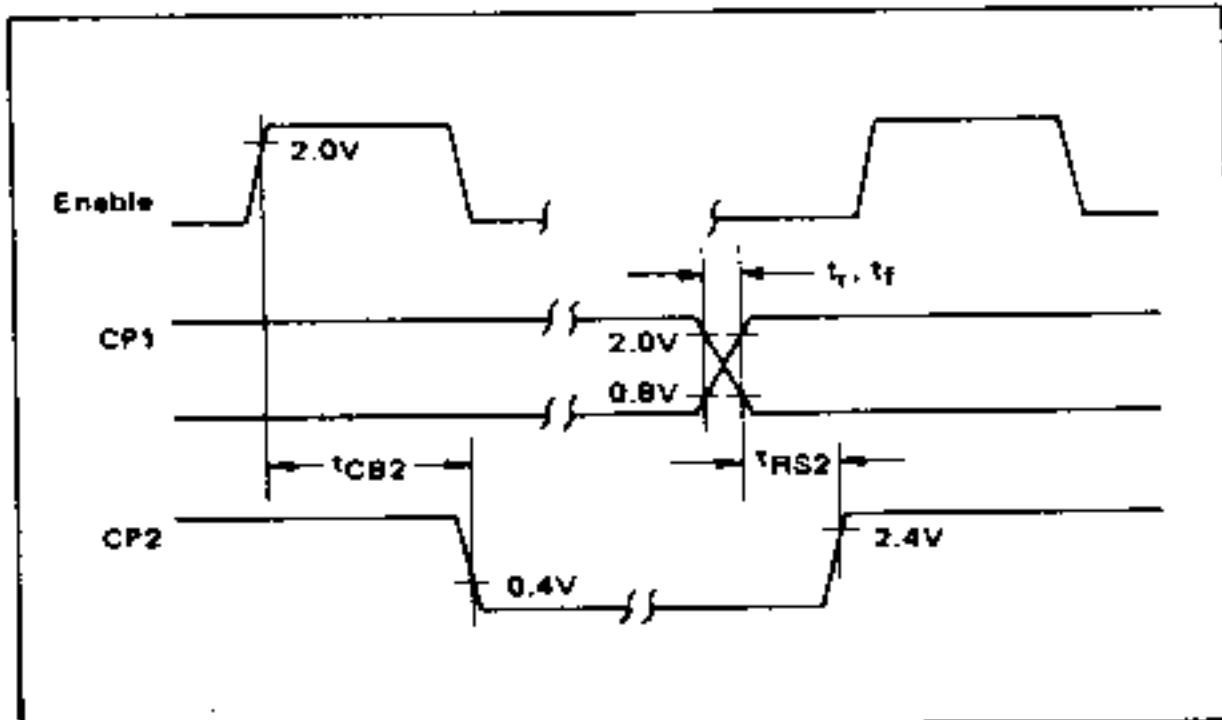
FIGURE 10 — INPUT PULSE WIDTHS
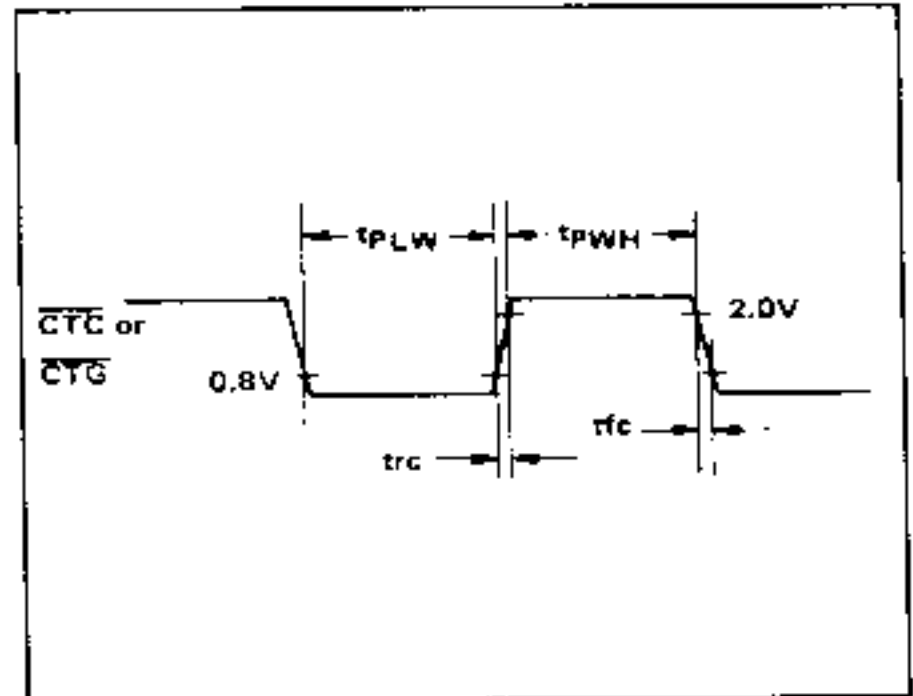
FIGURE 11 — INPUT SET-UP AND HOLD TIMES

NOTE: This mode is valid only for synchronous operation.
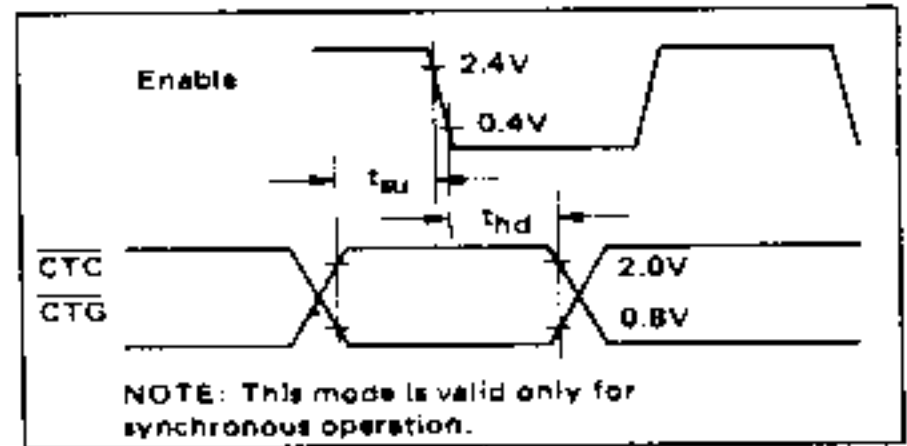
FIGURE 12 — OUTPUT DELAY

FIGURE 13 — BUS TIMING TEST LOADS

Load A
(D0-D7, CTO, CP2, PP0-PP7)

R_L = 2.5 k

Test Point

MMD6150 or Equiv.

MMD7000 or Equiv.

Load B
(IRQ Only)

3 k

Test Point

100 pF

C = 130 pF for D0-D7
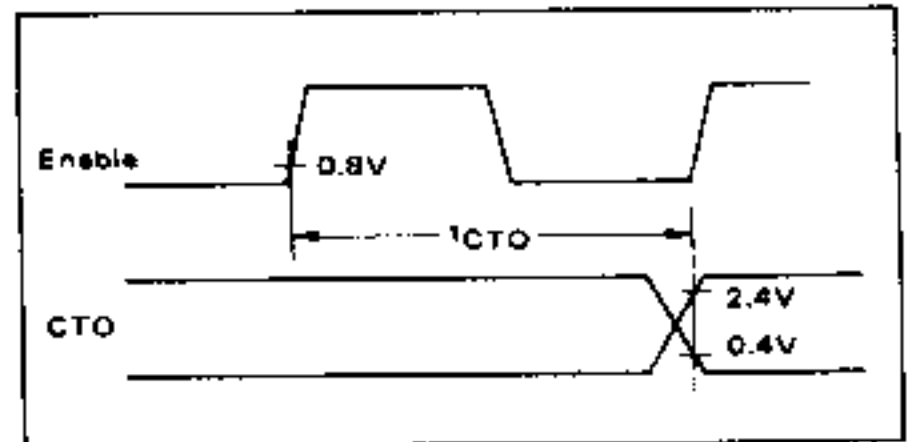 = 30 pF for CTO, CP2, PP0-PP7
R = 11.7 kΩ for D0-D7
  = 24 kΩ for CTO, CP2, PP0-PP7
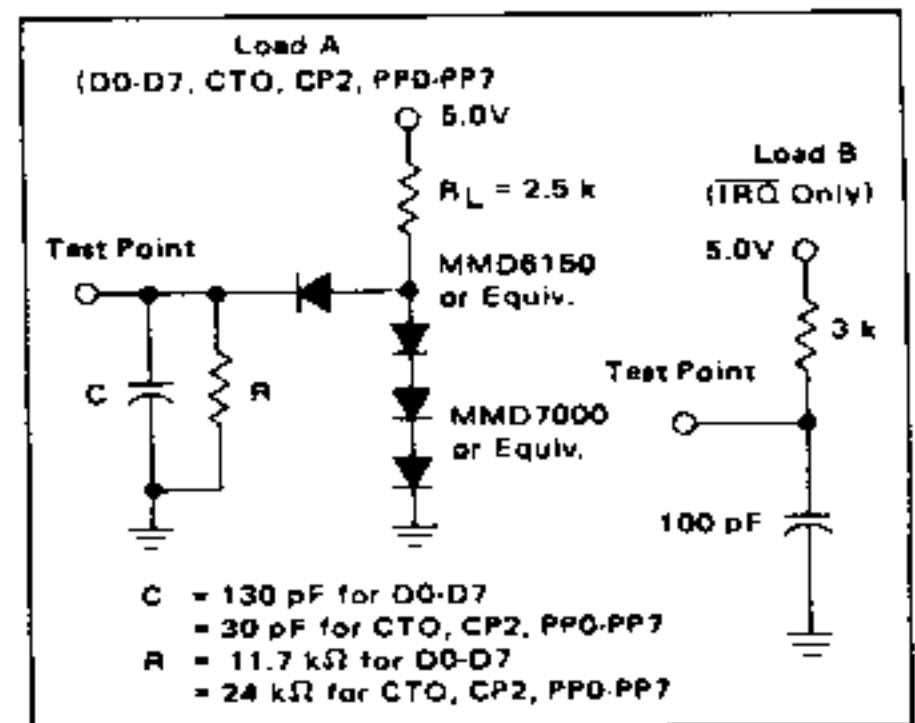
SIGNAL DESCRIPTION

BUS INTERFACE

The MC6846 interfaces to the M6800 Bus via an eight-bit bidirectional data bus, two Chip Select lines, a Read/Write line, and eleven address lines. These signals, in conjunction with the M6800 VMA output, permit the MPU to control the MC6846.

BIDIRECTIONAL DATA BUS (D0-D7)

The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the MC6846. The data bus output drivers are three-state devices which remain in the high-impedance (Off) state except when the MPU performs an MC6846 register or ROM read (R/$\overline{W}$ = 1 and I/O Registers or ROM selected).

CHIP SELECT (CS0, CS1)

The CS0 and CS1 inputs are used to select the ROM or I/O timer of the MC6846. They are mask programmed to be active high or active low as chosen by the user.

ADDRESS INPUTS (A0-A10)

The Address Inputs allow any of the 2048 bytes of ROM to be uniquely selected when the circuit is operating in the ROM mode. In the I/O-Timer mode, address inputs A0, A1, and A2 select the proper I/O Register, while A3 through A10 (together with CS0 and CS1) can be used as additional qualifiers in the I/O Select circuitry. (See the section on I/O-Timer Select for additional details.)

$\overline{\text{RESET}}$

The active low state of the $\overline{\text{Reset}}$ input is used to initialize all register bits in the I/O section of the device to their proper values. (See the section on Initialization for Reset conditions for timer and peripheral registers.)

ENABLE (ϕ2)

This signal synchronizes data transfer between the MPU and the MC6846. It also performs an equivalent synchronization function on the external clock, reset, and gate inputs of the MC6846 Timer section.

READ/WRITE (R/$\overline{W}$)

This signal is generated by the MPU and is used to control the direction of data transfer on the bidirectional data pins. A low level on the R/$\overline{W}$ input enables the MC6846 input buffers and data is transferred to the circuit during the ϕ2 pulse when the part has been selected. A high level on the R/$\overline{W}$ input enables the output buffers and data is transferred to the MPU during ϕ2 when the part is selected.

INTERRUPT REQUEST ($\overline{\text{IRQ}}$)

The active low $\overline{\text{IRQ}}$ output acts to interrupt the MPU through logic included on the MC6846. This output utilizes an open drain configuration and permits other interrupt request outputs from other circuits to be connected in a wire-OR configuration.

PERIPHERAL DATA (P0-P7)

The peripheral data lines can be individually programmed as either inputs or outputs via the Data Direction Register. When programmed as outputs, these lines will drive two standard TTL loads (3.2 mA). They are also capable of sourcing up to 1.0 mA at 1.5 Volts (Logic "1" output.)

When programmed as inputs, the output drivers associated with these lines enter a three-state (high impedance) mode. Since there is no internal pull-up for these lines, they represent a maximum 10µA load to the circuitry driving them — regardless of logic state.

A logic zero at the $\overline{\text{Reset}}$ input forces the peripheral data lines to the input configuration by clearing the Data Direction Register. This allows the system designer to preclude the possibility of having a peripheral data output connected to an external driver output during power-up sequence.

INTERRUPT INPUT (CP1)

Peripheral input line CP1 is an input-only that sets the Interrupt Flags of the Composite Status register. The active transition for this signal is programmed by the peripheral control register for the parallel port. CP1 may also act as a strobe for the peripheral data register when it is used as an input latch. Details for programming CP1 are in the section on the parallel peripheral port.

PERIPHERAL CONTROL (CP2)

Peripheral Control line CP2 may be programmed to act as an Interrupt input or Peripheral Control output. As an input, this line has high impedance and is compatible with standard TTL voltage levels. As an output, it is also TTL compatible and may be used as a source of 1 mA at 1.5 V to directly drive the base of a Darlington transistor switch. This line is programmed by the Peripheral Control Register.

COUNTER TIMER OUTPUT (CTO)

The Counter Timer Output is software programmable by selected bits in the timer/counter control register. The mode of operation is dependent on the Timer control register, the gate input, and the clock source. The output is TTL compatible.

EXTERNAL CLOCK INPUT ($\overline{\text{CTC}}$)

Input pin $\overline{\text{CTC}}$ will accept asynchronous TTL voltage level signals to be used as a clock to decrement the Timer. The high and low levels of the external clock must be stable for at least one system clock period plus the sum of
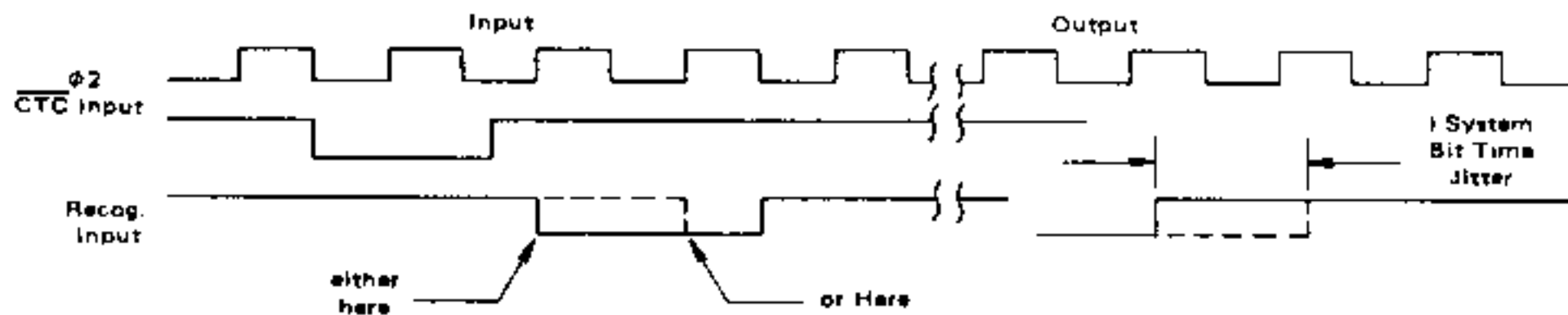
the setup and hold times for the inputs. The asynchronous clock rate can vary from dc to the limit imposed by System $\phi2$, setup, and hold times.

The external clock input is clocked in by Enable (System $\phi2$) pulses. Three Enable periods are used to synchronize and process the external clock. The fourth Enable pulse decrements the internal counter. This does not affect the input frequency; it merely creates a delay between a clock input transition and internal recognition of that transition by the MC6846. All references to $\overline{CTC}$ inputs in this document relate to internal recognition of the input transition. Note that a clock transition which does not meet setup and hold time specifications may require an additional Enable pulse for recognition.

When observing recurring events, a lack of synchronization will result in either "System jitter" or "Input jitter" being observed on the output of the MC6846 when using an asynchronous clock and gate input signal. "System jitter" is the result of the input signals being out of synchronization with the system $\phi2$ clock (Enable), permitting signals with marginal set-up and hold time to be recognized by either the bit time nearest the input

transition or subsequent bit time. "Input jitter" can be as great as the time between the negative going transitions of the input signal plus the system jitter if the first transition is recognized during one system cycle, and not recognized the next cycle or vice-versa.

GATE INPUTS ($\overline{CTG}$)

The input pin $\overline{CTG}$ accepts an asynchronous TTL-compatible signal which is used as a trigger or a clock gating function to the Timer. The gating input is clocked into the MC6846 by the Enable (System $\phi2$) signal in the same manner as the previously discussed clock inputs. That is, a $\overline{CTG}$ transition is recognized on the fourth Enable pulse (provided setup and hold time requirements are met), and the high or low levels of the $\overline{CTG}$ input must be stable for at least one system clock period plus the sum of setup and hold times. All references to $\overline{CTG}$ transition in this document relate to internal recognition of the input transition.

The $\overline{CTG}$ input of the timer directly affects the internal 16-bit counter. The operation of $\overline{CTG}$ is therefore independent of the $\div$ 8 prescaler selection.

FUNCTIONAL SELECT CIRCUITRY

I/O-TIMER SELECT CIRCUITRY

CS0 and CS1 are user programmable. Any of the four binary combinations of CS0 and CS1 can be used to select the ROM. Likewise, any other combination can be used to select the I/O-Timer. In addition, several address lines are used as qualifiers for the I/O-Timer. Specifically, A3 = A4 = A5 = logical "0". A6 can be programmed to a "1", "0", or don't care. A7 = A8 = A9 = A10 = don't care or one line only may be programmed to a logical "1". Figure 14 outlines in diagrammatic form the available chip select options.

INTERNAL ADDRESSING

Seven I/O Register locations within the MC6846 are accessible to the MPU data bus. Selection of these registers is controlled by A0, A1, and A2 (as shown in Table 1) provided the I/O timer is selected. The combination status register is Read-only; all other Registers are Read and Write.

TABLE 1 — INTERNAL REGISTER ADDRESSES

REGISTER SELECTED	A2	A1	A0
Combination Status Register	0	0	0
Peripheral Control Register	0	0	1
Data Direction Register	0	1	0
Peripheral Data Register	0	1	1
Combination Status Register	1	0	0
Timer Control Register	1	0	1
Timer MSB Register	1	1	0
Timer LSB Register	1	1	1
ROM Address	x	x	x

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FIGURE 14 — I/O-TIMER SELECT CIRCUITRY
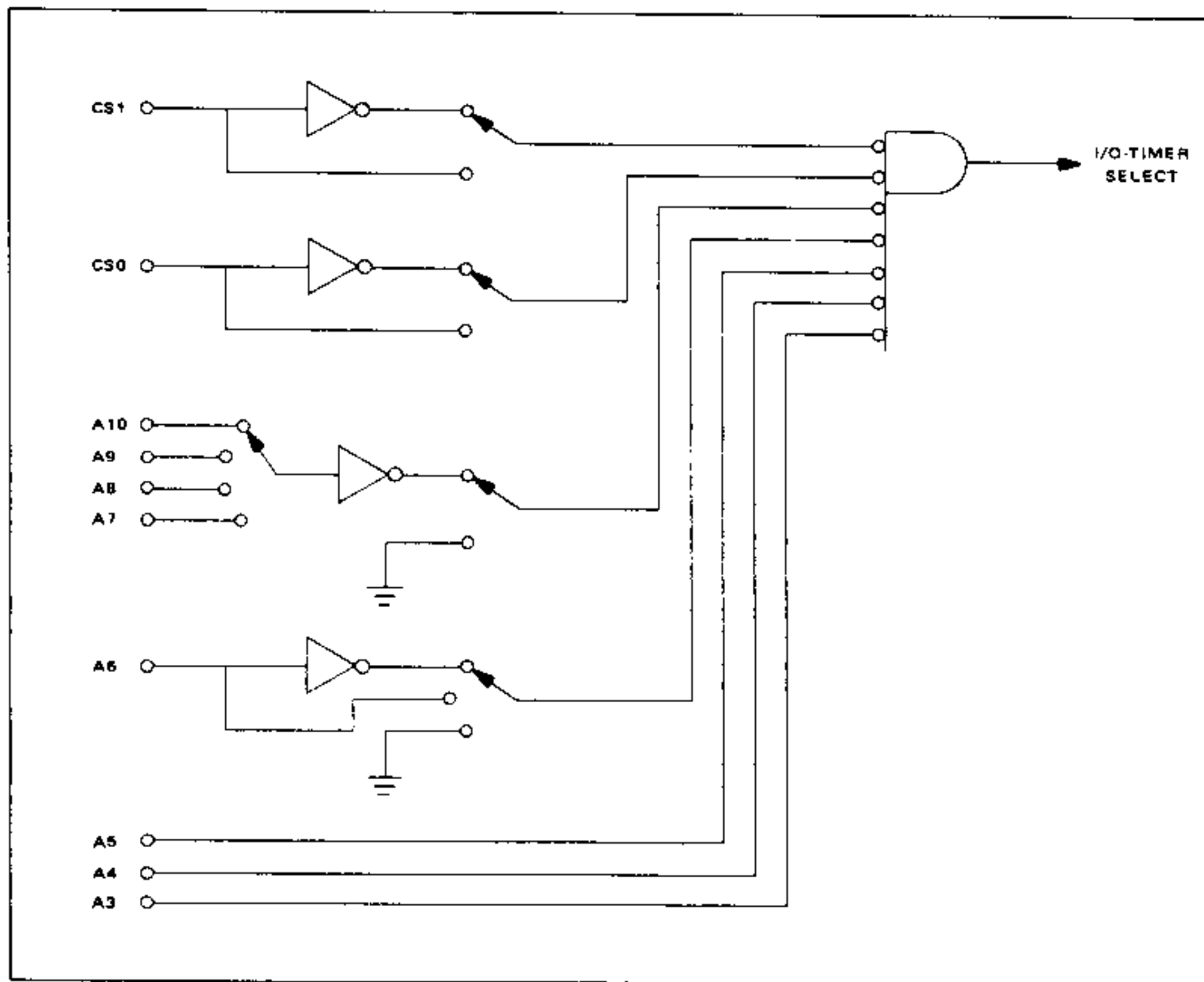
Initialization

When the $\overline{\text{Reset}}$ input has accepted a low signal, all registers are initialized to the reset state. The data direction and peripheral data registers are cleared. The Peripheral Control Register is cleared except for bit 7 (the $\overline{\text{Reset}}$ bit). This forces the parallel port to the input mode with interrupts disabled. To remove the $\overline{\text{Reset}}$ condition from the parallel port, a "0" must be written into the Peripheral Control Register bit 7 (PCR7).

The counter latches are preset to their maximal count, the Timer control register bits are reset to zero except for Bit 0 (TCR0 is set), the counter output is cleared, and the counter clock disabled. This state forces the timer counter to remain in an inactive state. The combination status register is cleared of all interrupt flags. During timer initialization, the reset bit (CCR0) must be cleared.

ROM

The Mask Programmable ROM section is similar in operation to other ROM products of the M6800 Microprocessor family. The ROM is organized as 2048 words of 8-bits to provide read-only storage for a minimum microcomputer system. The ROM is active when selected by the unique combination of the chip select inputs.

ROM Select

The active levels of CS0 and CS1 for ROM and I/O select are a user programmable option. Either CS0 or CS1 may be programmed active hi or active low, but different codes must be used for ROM or I/O select. CS0 and CS1 are mask programmed simultaneously with the ROM pattern. The ROM Select Circuitry is shown in Figure 15.

FIGURE 15 — ROM SELECT CIRCUITRY
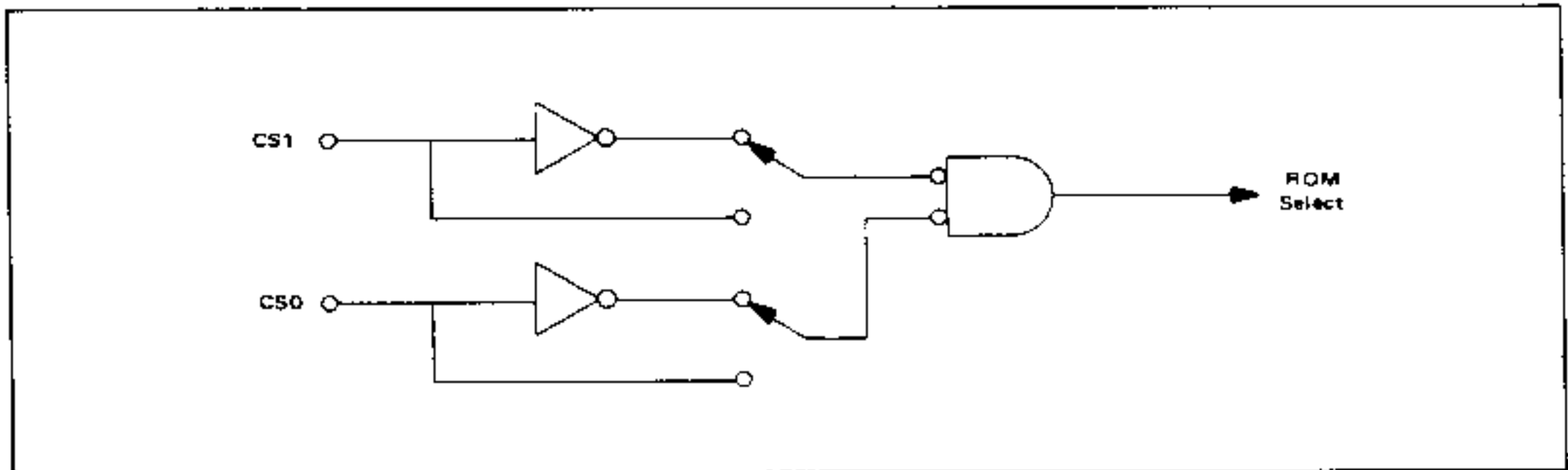
TIMER OPERATION

The Timer may be programmed to operate in modes which fit a wide variety of applications. The device is fully bus compatible with the M6800 system, and is accessed by Load and Store operations from the MPU.

In a typical application, the timer will be loaded by storing two bytes of data into the counter latch. This data is then transferred into the counter during a Counter Initialization cycle. The counter decrements on each subsequent clock cycle (which may be system $\phi2$ or an external clock) until one of several predetermined conditions causes it to halt or recycle. Thus the timer is programmable, cyclic in nature, controllable by external inputs or MPU program, and accessible to the MPU at any time.

COUNTER LATCH INITIALIZATION

The Timer consists of a 16-bit addressable counter and two 8 bit addressable latches. The function of the latches is to store a binary equivalent of the desired count value minus one. Counter initialization results in the transfer of the latch contents of the counter. It should be noted that data transfer to the counters is always accomplished via the latches. Thus, the counter latches may be accurately described as a 16-bit "counter initialization data" storage register.

In some modes of operation, the initialization of the latches will cause simultaneous counter initialization (i.e. immediate transfer of the new latch data into the counters). It is, therefore, necessary to insure that all 16 bits of the latches are updated simultaneously. Since the MC6846 data bus is 8 bits wide, a temporary register (MSB Buffer Register) is provided for in the Most Significant Byte of the desired latch data. This is a "write-only" register selected via address lines A0, A1, and A2. Data is transferred directly from the data bus to the MSB Buffer when the chip is selected, R/$\overline{W}$ is low, and the timer MSB register is selected (A0 = "0"; A1 = A2 = "1").

The lower 8 bits of the counter latch can also be referred to as a "write-only" register. Data Bus information will be transferred directly to the LSB of a counter latch when the chip is selected, R/$\overline{W}$ is low and the Timer LSB Register is selected (A0 = A1 = A2 = "1"). Data from the MSB Buffer will automatically be transferred into the Most Significant Byte of the counter latches simultaneously with the transfer of the Data Bus information to the Least Significant Byte of the Counter Latch. For brevity, the conditions for this operation will be referred to henceforth as a "Write Timer Latches Command."

The MC6846 has been designed to allow transfer of two bytes of data into the counter latches from any source, provided the MSB is transferred first. In many applications, the source of data will be an M6800 MPU. It should therefore be noted that the 16-bit store operations of the M6800 family microprocessors (STS and STX) transfer data in the order required by the MC6846. A Store Index Register instruction, for example, results in the MSB of the X register being transferred to the selected address, then the LSB of the X register being written into the next higher location. Thus, either the index register or stack pointer may be transferred directly into a selected counter latch with a single instruction.

A logic zero at the $\overline{\text{Reset}}$ input also initializes the counter latches. All latches will assume maximum count (65, 535) values. It is important to note that an internal Reset (Bit zero of the Timer/Control Register Set) has no effect on the counter latches.

COUNTER INITIALIZATION

Counter Initialization is defined as the transfer of data from the latches to the counter with attendant clearing of the Individual Interrupt Flag associated with the counter. Counter Initialization always occurs when a reset condition (external $\overline{\text{Reset}}$ = 0 or TCR0 = 1) is recognized. It can also occur (dependent on The Timer Mode) with a

Write Timer Latches command or recognition of a negative transition of the $\overline{\text{Gate}}$ input.

Counter recycling or reinitialization occurs when a clock input is recognized after the counter has reached an all-zero state. In this case, data is transferred from the Latches to the Counter, but the Interrupt Flag is unaffected.

TIMER CONTROL REGISTER

The Timer Control register (see Table 2) in the MC6846 is used to modify timer operation to suit a variety of applications. The Timer Control Register has a unique address space (A0 = 1, A1 = 0, A2 = 1) and therefore may be written into at any time. The least significant bit of the Control Register is used as an Internal Reset bit. When this bit is a logic zero, all timers are allowed to operate in the modes prescribed by the remaining bits of the timer control register.

Writing "one" into **Timer Control Register Bit 0** (TCR0) causes the counter to be preset with the contents of the counter latches, all counter clocks are disabled, and the timer output and interrupt flag (Status Register) are reset. The Counter Latch and Timer/Control Register are undisturbed by an Internal Reset and may be written into regardless of the state of TCR0.

Timer Control Register Bit 1 (TCR1) is used to select the clock source. When TCR1 = 0, the external clock input $\overline{\text{CTC}}$ is selected, and when TCR1 = "1", the timer uses system $\phi2$.

Timer Control Register Bit 2 (TCR2) enables the $\div 8$ prescaler (TCR2 = "1"). In this mode, the clock frequency is divided by eight before being applied to the counter. When TCR2 = "0" the system clock is applied directly to the counter.

TCR3, 4, 5 select the Timer Operating Mode, and are discussed in the next section.

Timer Control Register Bit 6 (TCR6) is used to mask or enable the Timer Interrupt Request. When TCR6 = 0, the Interrupt Flag is masked from the timer. When TCR6 = 1, the Interrupt Flag is enabled into Bit 7 of the Composite Status Register (Composite IRQ Bit), which appears on the $\overline{\text{IRQ}}$ output pin.

Timer Control Register Bit Seven (TCR7) has a special function when the timer is in the Cascaded Single Shot mode. (This function is explained in detail in the section describing the mode.) In all other modes, TCR7 merely acts as an output enable bit. If TCR7 = 0, the Counter Timer Output (CTO) is forced low. Writing a logic one into TCR7 enables CTO.

TIMER OPERATING MODES

The MC6846 has been designed to operate effectively in a wide variety of applications. This is accomplished by using three bits of the control register (TCR3, TCR4, and TCR5) to define different operating modes of the Timer, outlined in Table 3.

TABLE 2 — FORMAT FOR TIMER/COUNTER CONTROL REGISTER

CONTROL REGISTER BIT	STATE	BIT DEFINITION	STATE DEFINITION
TCR0	0	Internal Reset	Timer Enabled
	1		Timer in Preset State
TCR1	0	Clock Source	Timer uses External Clock ($\overline{\text{CTC}}$)
	1		Timer uses $\phi2$ System Clock
TCR2	0	$\div 8$ Prescaler	Clock is not Prescaled
	1	Enabler	Clock is prescaled by $\div 8$ Counter
TCR3 TCR4 TCR5	X X X	Operating Mode Selection	See Table 3
TCR6	0	Timer Interrupt	$\overline{\text{IRQ}}$ Masked from Timer
	1	Enable	$\overline{\text{IRQ}}$ Enabled from Timer
TCR7	0	Timer Output Enable	Counter Output (CTO) Set LOW
	1		Counter Output Enabled

TABLE 3 — OPERATING MODES

TCR3	TCR4	TCR5	Timer Operating Mode	Counter Initialization	Interrupt Flag Set
0	0	0	Continuous	$\overline{CTG}\downarrow + W + R$	T.O.
0	0	1	Cascaded Single Shot	$\overline{CTG}\downarrow + R$	T.O.
0	1	0	Continuous	$\overline{CTG}\downarrow + R$	T.O.
0	1	1	Normal Single Shot	$\overline{CTG}\downarrow + R$	T.O.
1	0	0	Frequency Comparison	$\overline{CTG}\downarrow \cdot \overline{I} \cdot (W + T.O.) + R$	$\overline{CTG}\downarrow$ Before T.O.
1	0	1		$\overline{CTG}\downarrow \cdot \overline{I} + R$	T.O. Before $\overline{CTG}\downarrow$
1	1	0	Pulse Width Comparison	$\overline{CTG}\downarrow \cdot \overline{I} + R$	$\overline{CTG}\uparrow$ Before T.O.
1	1	1			T.O. Before $\overline{CTG}\uparrow$

R = Reset Condition
W = Write Timer Latches
T.O. - Counter Time Out

$\overline{CTG}\downarrow$ = Negative Transition of Pin 17
$\overline{CTG}\uparrow$ = Positive Transition of Pin 17
$\overline{I}$ = Interrupt Flag (CSR0) = 0

CONTINUOUS OPERATING MODE (TCR3 = 0, TCR5 = 0)

The timer may be programmed to operate in a continuous counting mode by writing zeros into bits 3 and 5 of the timer control register. Assuming that the timer output is enabled (TCR7 = 1), a square wave will be generated at the Timer Output CTO (see Table 4).

Either a Timer Reset (TCR0 = 1 or External $\overline{Reset}$ = 0) condition or internal recognition of a negative transition of the $\overline{CTG}$ input results in Counter Initialization. A Write Timer Latches command can be selected as a Counter Initialization signal by clearing TCR4.

The discussion of the Continuous Mode has assumed the application requires an output signal. It should be noted the Timer operates in the same manner with the output disabled (TCR7 = 0). A Read Timer Counter command is valid regardless of the state of TCR7.

NORMAL SINGLE-SHOT TIMER MODE (TCR3 = 0, TCR4 = 1, TCR5 = 1)

This mode is identical to the Continuous Mode with two exceptions. The first of these is obvious from the name - the output returns to a low-level after the initial Time Out and remains low until another Counter Initialization cycle occurs. The output waveform (CTO) is shown in Figure 16.

As indicated in Figure 16, the internal counting mechanism remains cyclical in the Single-Shot Mode. Each Time Out of the counter results in the setting of an Individual Interrupt Flag and re-initialization of the counter.

The second major difference between the Single-Shot and Continuous modes is that the internal counter enable is not dependent on the $\overline{CTG}$ input level remaining in the low state for the Single-Shot mode. Aside from these differences, the two modes are identical.

TABLE 4 — CONTINUOUS OPERATING MODES

CONTINUOUS MODE (TCR3 = 0, TCR7 = 1, TCR5 = 0)				
CONTROL REGISTER	INITIALIZATION/OUTPUT WAVEFORMS			
TCR2	TCR4	Counter	Timer Output (2X)	
0	0	Initialization $\overline{CTG}\downarrow + \overline{W} + R$	$\leftarrow(N+1)(T)\rightarrow \leftarrow(N+1)(T)\rightarrow \leftarrow(N+1)(T)\rightarrow$	V_{OH} / V_{OL}
0	1	$\overline{CTG}\downarrow + R$	to T.O. T.O. T.O.	

$\overline{CTG}$ = Negative Transition $\overline{GATE}$ Input.
$\overline{W}$ = Write Timer Latches Command.
R = Timer Reset (TCR0 = 1 or External $\overline{RESET}$ = 0)
N = 16 Bit Number in Counter Latch.

T = Period of Clock Input to Counter.
to - Counter Initialization Cycle.
T.O. = Counter Time Out (All Zero Condition).

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FIGURE 16 – SINGLE-SHOT MODES
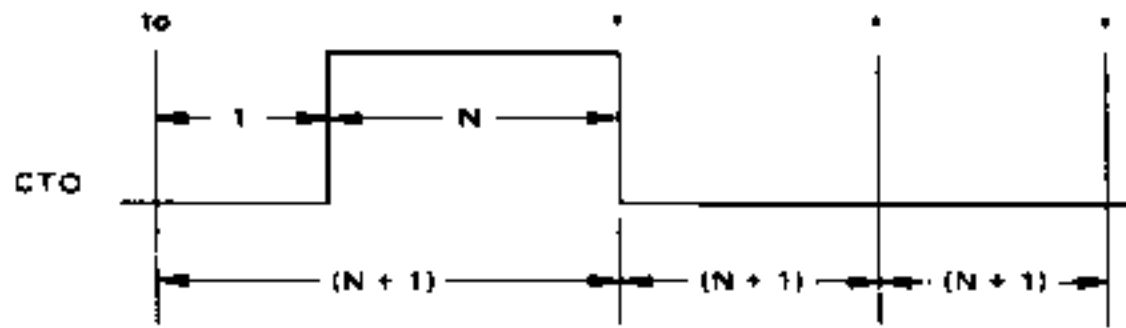
(A) NORMAL SINGLE-SHOT MODE OUTPUT WAVEFORM

(B) CASCADED SINGLE-SHOT MODE OUTPUT WAVEFORM

1 = Write a "1" into TCR-7
0 = Write a "0" into TCR-7

*POINT AT WHICH AN INTERRUPT MAY OCCUR

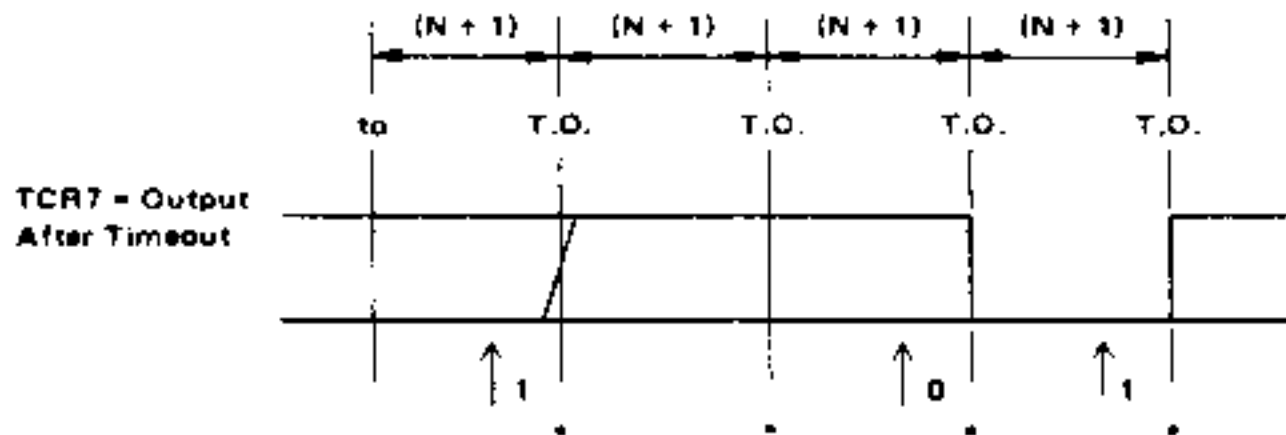Note: All time intervals shown above assume the Gate ($\overline{CTG}$) and Clock ($\overline{CTC}$) signals are synchronized to system $\phi2$ with the specified setup and hold time requirements.

TIME INTERVAL MODES (TCR3 = 1)

The Time Interval Modes are provided for applications requiring more flexibility of interrupt generation and Counter Initialization. The Interrupt Flag is set in these modes as a function of both Counter Time Out and transitions of the $\overline{CTG}$ input. Counter Initialization is also affected by Interrupt Flag status. The output signal is not defined in any of these modes. Other features of the Time Interval Modes are Outlined in Table 5.

TABLE 5 – TIME INTERVAL MODES

TCR3 = 1			
TCR4	TCR5	APPLICATION	CONDITION FOR SETTING INDIVIDUAL INTERRUPT FLAG
0	0	Frequency Comparison	Interrupt Generated if $\overline{CTG}$ Input Period (1/F) is Less Than Counter Time Out (T.O.)
0	1	Frequency Comparison	Interrupt Generated if $\overline{CTG}$ Input Period (1/F) is Greater Than Counter Time Out (T.O.)
1	0	Pulse Width Comparison	Interrupt Generated If $\overline{CTG}$ Input "Down Time" is Less Than Counter Time Out (T.O.)
1	1	Pulse Width Comparison	Interrupt Generated if $\overline{CTG}$ Input "Down Time" is Greater Than Counter Time Out (T.O.)

CASCADED SINGLE-SHOT MODE
(TCR3 = 0, TCR4 = 0, TCR5 = 1)

This mode is identical to the single-shot mode with two exceptions. First, the output waveform does not return to a low level and remain low after timeout. Instead, the output level remains at its initialized level until it is re-programmed and changed by timeout. The output level may be changed at any timeout or may have any number of timeouts between changes.

The second difference is the method used to change the output level. Timer Control Register Bit 7 (TCR7) has a special function in this mode. The timer output (CTO) is equal to TCR7 clocked by timeout. At every timeout, the content of TCR7 is clocked to and held at the CTO output. Thus, output pulses of length greater than one timer cycle can be generated by cascading timer cycles and counting timeouts with a software program. (See Figure 16).

An interrupt is generated at each timeout. To cascade timer cycles, the MPU would need an interrupt routine to: 1) count each timeout and determine when to change TCR7; 2) write into TCR7 the state corresponding to the next desired state of the output waveform (only necessary during the last timer cycle before the output is to change state); and 3) clear the interrupt flag by reading the combination status register followed by Read Timer MSB. It is also possible, if desired, to change the length of the timer cycle by reinitializing the timer latches. This allows more flexibility for obtaining desired times.

FREQUENCY COMPARISON MODE
(TCR3 = 1, TCR4 = 0)

The timer within the MC6846 may be programmed to compare the period of a pulse (giving the frequency after calculations) at the $\overline{CTG}$ input with the time period required for Counter Time Out. A negative transition of the $\overline{CTG}$ input enables the counter and starts a Counter Initialization cycle — provided that other conditions as noted in Table 6 are satisfied. The counter decrements on each clock signal recognized during or after Counter Initialization until an Interrupt is generated, a Write Timer Latches command is issued, or a Timer Reset condition occurs. It can be seen from Table 6 that an interrupt condition will be generated if TCR5 = 0 and the period of the pulse (single pulse or measured separately repetitive pulses) at the $\overline{CTG}$ input is less than the Counter Time Out period. If TCR5 = 1, an interrupt is generated if the reverse is true.

Assume now with TCR5 = 1 that a Counter Initialization has occurred and that the $\overline{CTG}$ input has returned low prior to Counter Time Out. Since there is no Individual Interrupt Flag generated, this automatically starts a new Counter Initialization Cycle. The process will continue with frequency comparison being performed on each $\overline{CTG}$ input cycle until the mode is changed, or a cycle is determined to be above the predetermined limit.

PULSE WIDTH COMPARISON MODE
(TCR3 = 1, TCR4 = 1)

This mode is similar to the Frequency Comparison Mode except for the limiting factor being a positive, rather than negative, transition of the $\overline{CTG}$ input. With TCR5 = 0, an Individual Interrupt Flag will be generated if the zero level pulse applied to the $\overline{CTG}$ input is less than the time period required for Counter Time Out. With TCR5 = 1, the interrupt is generated when the reverse condition is true.

As can be seen in Table 7, a positive transition of the $\overline{CTG}$ input disables the counter. With TCR 5 = 0, it is therefore possible to directly obtain the width of any pulse causing an interrupt.

TABLE 6 — FREQUENCY COMPARISON MODE

CRX3 = 1, CRX4 = 0				
Control Reg Bit 5 (CRX5)	Counter Initialization	Counter Enable Flip-Flop Set (CE)	Counter Enable Flip-Flop Reset (CE)	Interrupt Flag Set (I)
0	$\overline{G}\downarrow\cdot\overline{I}\cdot(\overline{CE}+TO\cdot CE)+R$	$G\downarrow\cdot W\cdot\overline{R}\cdot\overline{I}$	$W+R+I$	$G\downarrow$ Before TO
1	$\overline{G}\downarrow\cdot\overline{I}+R$	$G\downarrow\cdot\overline{W}\cdot\overline{R}\cdot\overline{I}$	$W+R+I$	TO Before $G\downarrow$

I represents the interrupt for the timer.

TABLE 7 — PULSE WIDTH COMPARISON MODE

CRX3 = 1, CRX4 = 1				
Control Reg Bit 5 (CRX5)	Counter Initialization	Counter Enable Flip-Flop Set (CE)	Counter Enable Flip-Flop Reset (CE)	Interrupt Flag Set (I)
0	$\overline{G}\downarrow\cdot\overline{I}+R$	$G\downarrow\cdot W\cdot R\cdot I$	$W+R+I+G$	$\overline{G}\uparrow$ Before TO
1	$\overline{G}\downarrow\cdot\overline{I}+R$	$G\downarrow\cdot\overline{W}\cdot\overline{R}\cdot\overline{I}$	$W+R+I+G$	TO Before $\overline{G}\uparrow$

DIFFERENCES BETWEEN THE MC6840 AND THE MC6846 TIMERS

1) Control registers 1 and 3 are buried (access through control register 2 only) in the MC6840 timer. In the MC6846, all registers are directly accessible.

2) The MC6840 has a dual 8 bit continuous mode for generating non-symmetrical waveforms. The MC6846, instead, has a cascaded one shot mode which can accomplish the same function, but also allows the user to generate waveforms longer than one timeout.

3) Because of the different modes, there is a difference in the control registers between the MC6840 and the MC6846.

CONTROL REGISTER BIT	MC6840	MC6846
2	16 bit or dual 8 bit mode control	: 8 prescale enable
7	output enable (all modes)	output next state (cascaded one shot mode only), output enable all other modes
0	R₁ internal reset R₂ control register select R₃ timer 3 clock control	internal reset

COMPOSITE STATUS REGISTER

The Composite Status Register (CSR) is a read-only register which is shared by the Timer and the Peripheral Data Port of the MC6846. Three individual interrupt flags in the register are set directly via the appropriate conditions in the timer or peripheral port. The composite interrupt flag — and the $\overline{IRQ}$ Output — respond to these individual interrupts only if corresponding enable bits are set in the appropriate Control Registers. (See Figure 17.) The sequence of assertion is not detected. Setting TCR6 while CSR0 is high will cause CSR7 to be set, for example.

The Composite Interrupt Flag (CSR7) is clear only if all enabled Individual Interrupt Flags are clear. The conditions for clearing CSR1 and CSR2 are detailed in a later section. The Timer Interrupt Flag (CSR0) is cleared under the following conditions:

1) Timer Reset — Internal Reset Bit (TCR0) = 1 or External $\overline{Reset}$ = 0.

2) Any Counter Initialization condition.

3) A Write Timer Latches command if Time Interval modes (TCR3 = 1) are being used.

4) A Read Timer Counter command, provided this is preceded by a Read Composite Status Register while CSR0 is set. This latter condition prevents missing an Interrupt Request generated after reading the Status Register and prior to reading the counter.

The remaining bits of the Composite Status Register (CSR3-CSR6) are unused. They default to a logic zero when read.

FIGURE 17 — COMPOSITE STATUS REGISTER & ASSOCIATED LOGIC
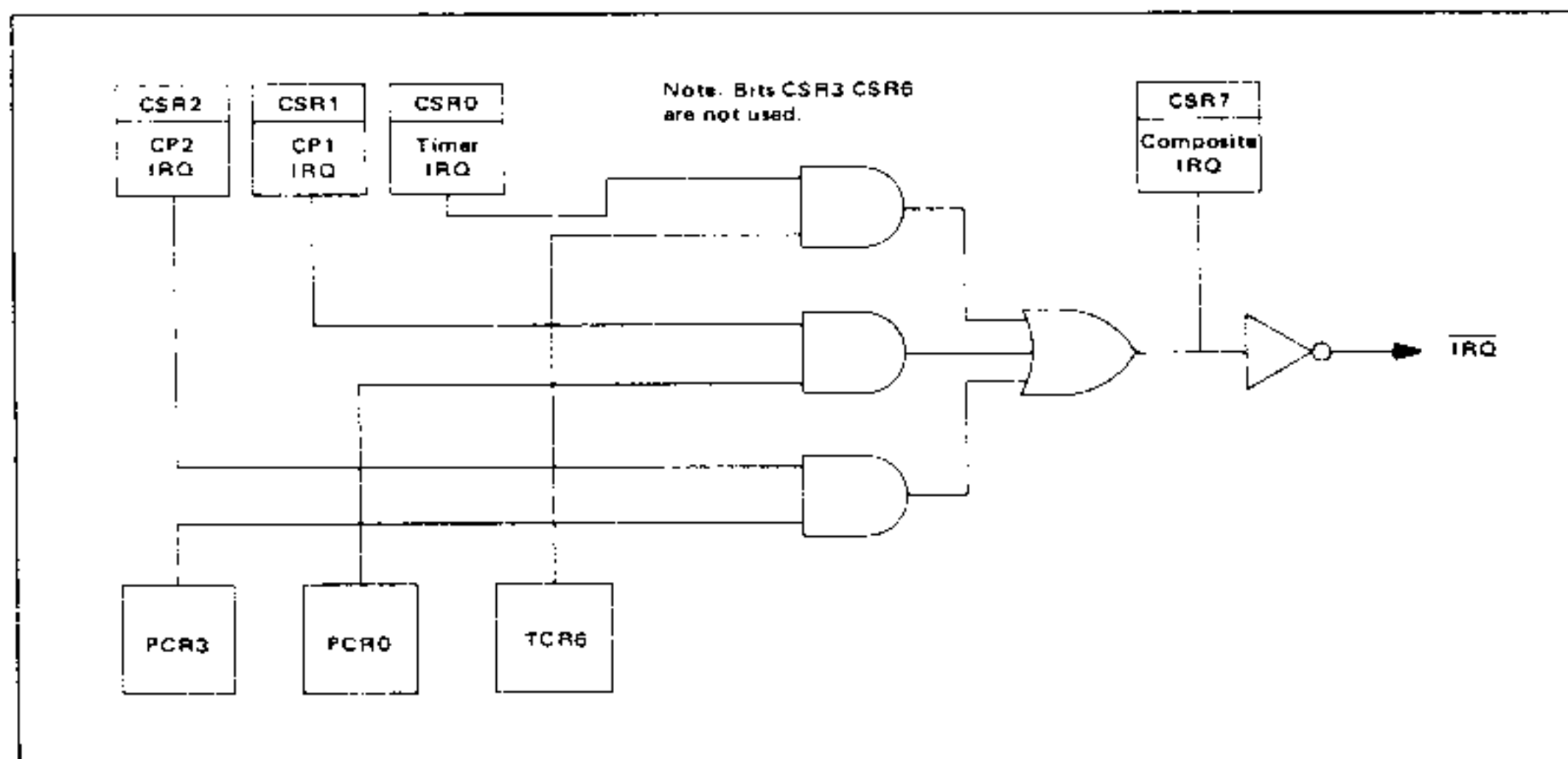
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I/O OPERATION

PARALLEL PERIPHERAL PORT

The peripheral port of the MC6846 contains 8 Peripheral Data lines (P0-P7), two Peripheral Control lines (CP1 and CP2), a Data Direction Register, a Peripheral Data Register, and a Peripheral Control Register. The port also directly affects two bits (CSR1 and CSR2) of the Composite Status Register.

The Peripheral Port is similar to the "B" side of a PIA (MC6820 or MC6821) with the following exceptions:

1) All registers are directly accessible in the MC6846. Data Direction and Peripheral Data in the MC6820/6821 are located at the same address, with Bit Two of the Control Register used for register selection.

2) Peripheral Control Register Bit Two (PCR2) of the MC6846 is used to select an optional input latch function. This option is not available with MC6820/6821 PIA's.

3) Interrupt Flags are located in the MC6846 composite status register rather than Bits 6 and 7 of the Control Register as used in the MC6820/6821.

4) Interrupt Flags are cleared in the MC6820/6821 by reading data from the Peripheral Data Register. MC6846 Interrupt Flags are cleared by either reading or writing to the Peripheral Data Register – provided that this sequence is followed a) Flag Set, b) Read Composite Status Register, c) Read/Write Peripheral Data Register is followed.

5) Bit 6 of the MC6846 Peripheral Control Register is not used. Bit 7 (PCR7) is an Internal Reset Bit not available on the MC6820/6821.

6) The Peripheral Data lines (and CP2) of the MC6846 feature internal current limiting which allows them to directly drive the base of Darlington NPN transistors.

DATA DIRECTION REGISTER

The MPU can write directly to this eight-bit register to configure the Peripheral Data lines as either inputs or outputs. A particular bit within the register (DDRN) is used to control the corresponding Peripheral Data line (PN). With DDRN = 0, PN becomes an input; if DDRN = 1, PN is an output. As an example, writing Hex $0F into the Data Direction Register results in P0 thru P3 becoming outputs and P4 thru P7 being inputs. Hex $55 in the Data Direction Register results in alternate outputs and inputs at the parallel port.

PERIPHERAL DATA REGISTER

This eight-bit register is used for transferring data between the peripheral data port and the MPU. Any bit corresponding to an output line will be used to drive the output buffer associated with that line. Data in these output bits is normally provided by an MPU Write function. (Input bits — those associated with input lines — are unchanged by a Write Command.) Any input bit will reflect the state of the associated input line if the input latch function is deselected. If the Control Register is programmed to provide input latching, the input bit will retain the state at the time CP1 was activated until the Peripheral Data Register is read by the MPU.

PERIPHERAL CONTROL REGISTER

This eight bit register is used to control the reset function as well as for selection of optional functions of the two peripheral control lines (CP1 and CP2). The Peripheral Control Register functions are outlined in Table 8.

TABLE 8 – PERIPHERAL CONTROL REGISTER FORMAT (Expanded)
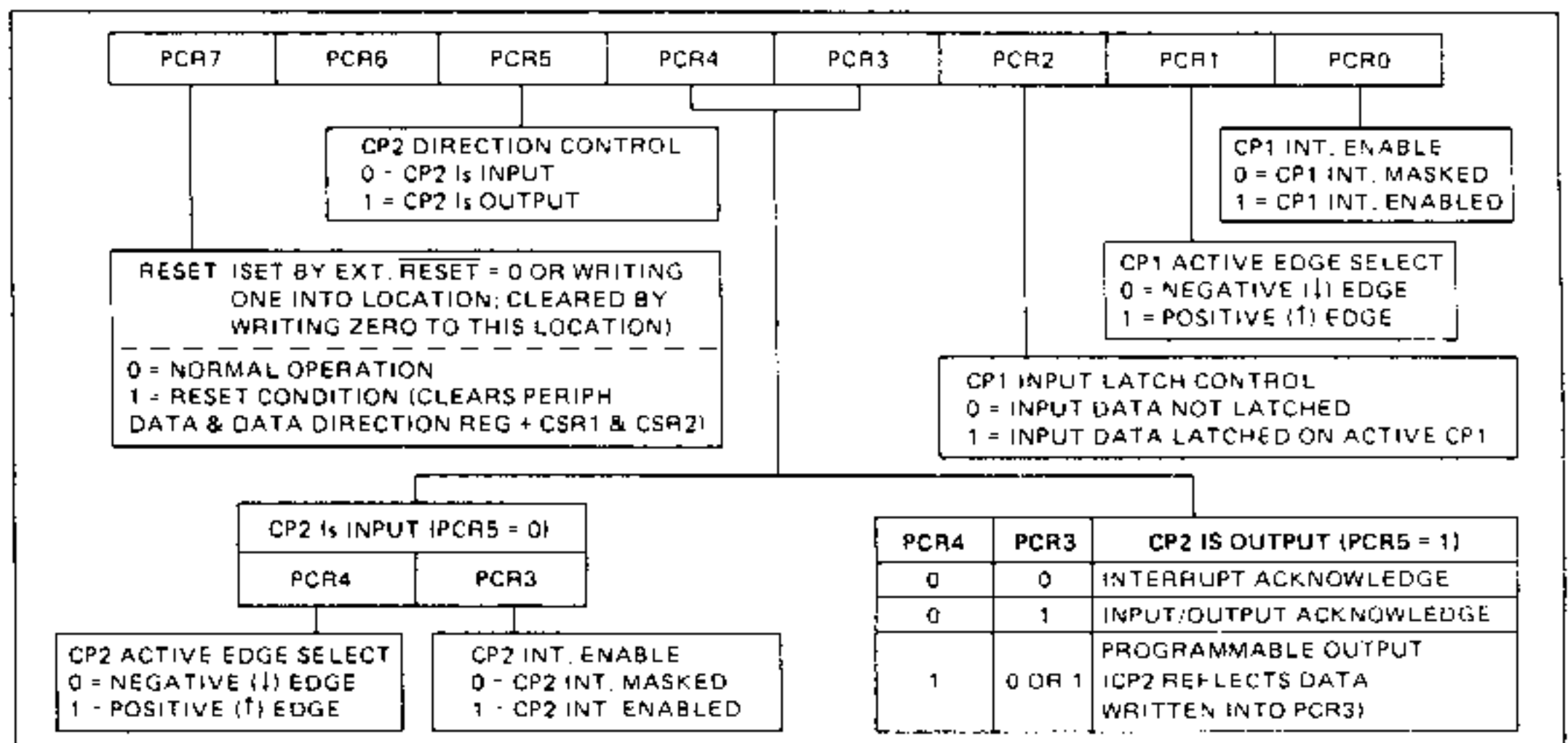
PERIPHERAL PORT RESET (PCR7)

Bit 7 of the Peripheral Control Register (PCR7) may be used to initialize the peripheral section of the MC6846. When this bit is set high, the peripheral data register, the peripheral data direction register, and the interrupt flags associated with the peripheral port (CSR1 & CSR2) are all cleared. Other bits in the peripheral control register are not affected by PCR7.

PCR7 is set by either a logic zero at the External RESET input or under program control by writing a "one" into the location. In any case, PCR7 may be cleared only by writing a zero into the location while RESET is high. The bit must be cleared to activate the port.

CONTROL OF CP1 PERIPHERAL CONTROL LINE

CP1 may be used as an interrupt request to the MC6846, as a strobe to allow latching of input data, or both. In any case, the input can be programmed to be activated by either a positive or negative transition of the signal. These options are selected via Control Register Bits PCR0, PCR1 & PCR2

Control Register Bit 0 (PCR0) is used to enable the interrupt transfer circuitry of the MC6846. Regardless of the state of PCR0, an active transition of CP1 causes the Composite Status Register Bit One (CSR1) to be set. If PCR0 = 1, this interrupt will be reflected in the Composite Interrupt Flag (CSR7), and thus at the IRQ output. CSR1 is cleared by a Peripheral Port Reset condition or by either reading or writing to the peripheral data register after the Composite Status Register is read. The latter alternative is conditional -- CSR1 must have been a logic one when the Composite Status Register was last read. This precludes inadvertent clearing of interrupt flags generated between the time the Status Register is read and the manipulation of peripheral data.

Control Register Bit One (PCR1) is used to select the edge which activates CP1. When PCR1 = 0, CP1 is active on negative transitions (high to low). Low to High transitions are sensed by CP1 when PCR1 = 1.

In addition to its use as an interrupt input, CP1 can be used as a strobe to capture input data in an internal latch. This option is selected by writing a one into Peripheral Control Register Bit Two (PCR2). In operation, the data at the pins designated by the Data Direction Register as inputs will be captured by an active transition of CP1. An MPU Read of the Peripheral Data Register will result in the captured data being transferred to the MPU -- and it also releases the latch to allow capture of new data. Note that successive active transitions with no Read Peripheral Data Command between does not update the input latch. Also, it should be noted that use of the input latch function (which can be deselected by writing a zero into PCR2) has no effect on output data. It also does not affect Interrupt function of CP1.

CONTROL OF CP2 PERIPHERAL CONTROL LINE

CP2 may be used as an input by writing a zero into PCR5. In this configuration, CP2 becomes a dual of CP1 in regard to generation of interrupts. An active transition (as selected by PCR4) causes Bit Two of the Composite Status Register to be set. PCR3 is then used to select whether the CP2 transition is to cause CSR7 to be set - and thereby cause IRQ to go low. CP2 has no effect on the input latch function of the MC6846.

Writing a one into PCR5 causes CP2 to function as an output. PCR4 then determines whether CP2 is to be used in a handshake or programmable output mode. With PCR4 = 1, CP2 will merely reflect the data written into PCR3. Since this can readily be changed under program control, this mode allows CP2 to be a programmable output line in much the same manner as those lines selected as outputs by the Data Direction Register.

The handshaking mode (PCR5 = 1, PCR4 = 0) allows CP2 to perform one of two functions as selected by PCR3. With PCR3 = 1, CP2 will go low on the first Enable (System φ2) positive transition after a Read or Write to the Peripheral Data Register. This Input/Output Acknowledge signal is released (returns high) on the next positive transition of the Enable signal.

In the Interrupt Acknowledge mode (PCR5 = 1, PCR4 = PCR3 = 0), CP2 is set when CSR1 is set by an active transition of CP1. It is released (goes low) on the first positive transition of Enable after CSR1 has been cleared via an MPU Read or Write to the Peripheral Data Register. (Note that the previously described conditions for clearing CSR1 still apply.)

RESTART SEQUENCE

A typical restart sequence for the MC6846 will include initialization of both the Peripheral Control & Data Direction Registers of the parallel port. It is necessary to set up the Peripheral Control Register first, since PCR7 = 0 is a condition for writing data into the Data Direction Register. (A logic zero at the external Reset input automatically sets PCR7.)

SUMMARY

The MC6846 has several optional modes of operation which allow it to be used in a variety of applications. The following tables are provided for reference in selecting these modes.

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TABLE 9 — MC6846 INTERNAL REGISTER ADDRESSES

A2	A1	A0	REGISTER SELECTED
0	0	0	Combination Status Register
0	0	1	Peripheral Control Register
0	1	0	Data Direction Register
0	1	1	Peripheral Data Register
1	0	0	Combination Status Register
1	0	1	Timer Control Register
1	1	0	Timer MSB Register
1	1	1	Timer LSB Register
X	X	X	ROM Address

TABLE 10 — COMPOSITE STATUS REGISTER

| CSR7 | CSR3-CSR6 NOT USED. DEFAULT TO ZERO WHEN READ | CSR2 | CSR1 | CSR0 |

COMPOSITE INTERRUPT FLAG
0 = NO ENABLED INTERRUPT FLAG SET
1 = ONE OR MORE ENABLED INTERRUPT FLAGS SET.*

INVERSE OF THIS BIT APPEARS AT $\overline{\text{IRQ}}$ OUTPUT

*STATUS OF THIS BIT CAN BE EXPRESSED AS:
CSR7 = CSR0 · TCR6 + CSR1 · PCR0 + CSR2 · PCR3

CP2 INTERRUPT FLAG
0 = NO INT REQ
1 = INT REQUESTED

TIMER INTERRUPT FLAG
0 = NO INT REQ.
1 = INT REQUESTED

CP1 INTERRUPT
0 = NO INT REQ.
1 = INT REQUESTED

TABLE 11 — TIMER CONTROL REGISTER

| TCR7 | TCR6 | TCR5 | TCR4 | TCR3 | TCR2 | TCR1 | TCR0 |

INTERRUPT ENABLE
0 = $\overline{\text{IRQ}}$ MASKED
1 = $\overline{\text{IRQ}}$ ENABLED

INTERNAL RESET
0 = TIMER ENABLED
1 = RESET STATE

TIMER OUTPUT ENABLE
0 = OUTPUT DISABLED (LOW)
1 = OUTPUT ENABLED

FOR CASCADED SINGLE-SHOT
0 = OUTPUT GOES LOW AT TIME OUT
1 = OUTPUT GOES HIGH AT TIME OUT

CLOCK SOURCE
0 = EXTERNAL CLOCK (CTC)
1 = INTERNAL CLOCK (ϕ2)

÷ 8 PRESCALE ENABLE
0 = CLOCK NOT PRESCALED
1 = CLOCK PRESCALED (÷ 8)

TCR3	TCR4	TCR5	TIMER OPERATING MODE	COUNTER INITIALIZATION	INTERRUPT FLAG SET
0	0	0	CONTINUOUS	$\overline{\text{CTG}}{\downarrow} + W + R$	T.O.
0	0	1	CASCADED SINGLE SHOT	$\overline{\text{CTG}}{\downarrow} + R$	T.O.
0	1	0	CONTINUOUS	$\overline{\text{CTG}}{\downarrow} + R$	T.O.
0	1	1	NORMAL SINGLE SHOT	$\overline{\text{CTG}}{\downarrow} + R$	T.O.
1	0	0	FREQUENCY COMPARISON	$\overline{\text{CTG}}{\downarrow} \cdot \overline{\text{I}} \cdot (W + \text{T.O.}) + R$	$\overline{\text{CTG}}{\downarrow}$ BEFORE T.O.
1	0	1		$\overline{\text{CTG}}{\downarrow} \cdot \overline{\text{I}} + R$	T.O. BEFORE $\overline{\text{CTG}}{\downarrow}$
1	1	0	PULSE WIDTH COMPARISON	$\overline{\text{CTG}}{\downarrow} \cdot \overline{\text{I}} + R$	$\overline{\text{CTG}}{\uparrow}$ BEFORE T.O.
1	1	1			T.O. BEFORE $\overline{\text{CTG}}{\uparrow}$

R = RESET CONDITION

W = WRITE TIMER LATCHES

T.O. = COUNTER TIME OUT

$\overline{\text{CTG}}{\downarrow}$ = NEG TRANSITION OF PIN 17

$\overline{\text{CTG}}{\uparrow}$ = POS TRANSITION OF PIN 17

$\overline{\text{I}}$ = INTERRUPT FLAG (CSR0) = 0

TABLE 12 – PERIPHERAL CONTROL REGISTER

PCR7	PCR6	PCR5	PCR4	PCR3	PCR2	PCR1	PCR0

CP2 DIRECTION CONTROL
0 = CP2 is INPUT
1 = CP2 is OUTPUT

CP1 INT. ENABLE
0 = CP1 INT. MASKED
1 = CP1 INT. ENABLED

RESET (SET BY EXT. RESET = 0 OR WRITING ONE INTO LOCATION; CLEARED BY WRITING ZERO TO THIS LOCATION)
0 = NORMAL OPERATION
1 = RESET CONDITION (CLEARS PERIPH DATA & DATA DIRECTION REG + CSR1 & CSR2)

CP1 ACTIVE EDGE SELECT
0 = NEGATIVE (↓) EDGE
1 = POSITIVE (↑) EDGE

CP1 INPUT LATCH CONTROL
0 = INPUT DATA NOT LATCHED
1 = INPUT DATA LATCHED ON ACTIVE CP1

CP2 Is INPUT (PCR5 = 0)

PCR4	PCR3

CP2 ACTIVE EDGE SELECT
0 = NEGATIVE (↓) EDGE
1 = POSITIVE (↑) EDGE

CP2 INT. ENABLE
0 = CP2 INT. MASKED
1 = CP2 INT. ENABLED

PCR4	PCR3	CP2 IS OUTPUT (PCR5 = 1)
0	0	INTERRUPT ACKNOWLEDGE
0	1	INPUT/OUTPUT ACKNOWLEDGE
1	0 OR 1	PROGRAMMABLE OUTPUT (CP2 REFLECTS DATA WRITTEN INTO PCR3)

CUSTOM PROGRAMMING

By the programming of a single photomask for the MC6846, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MC6846 should be submitted on an Organizational Data form such as that shown in Figure 18.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software
2. Hexadecimal coding using IBM Punch Cards.

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 2048 bytes.

Note. Motorola can accept magnetic tape and truth table formats. For further information, contact your local Motorola sales representative.

IBM PUNCH CARDS

The hexadecimal equivalent (from Table 13) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
	76	Blank
4	77-78	Card number (starting 01)
5	79-80	Total number of cards (32)

TABLE 13 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	F
1	1	1	1	F

FIGURE 18 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MC6846 COMBINATION ROM-I/O-TIMER

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.. _____

Enable Options: (ROM ENABLE MUST DIFFER FROM I/O-TIMER)

	1	0		1	0
CS0	☐	☐		☐	☐
CS1	☐	☐		☐	☐
ROM SECTION			I/O-TIMER SECTION		

	CHECK ONE COLUMN ONLY					
I/O-TIMER SELECT						1 ≥ 2.0V.
A6	A10	X	1	X	X	X	0 ≤ 0.8V.
1　0　X	A9	X	X	1	X	X	X -
☐　☐　☐	A8	X	X	X	1	X	NOT USED
	A7	X	X	X	X	1	

MC6846

P SUFFIX
PLASTIC PACKAGE
CASE 711-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "D").
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

L SUFFIX
CERAMIC PACKAGE
CASE 715-02
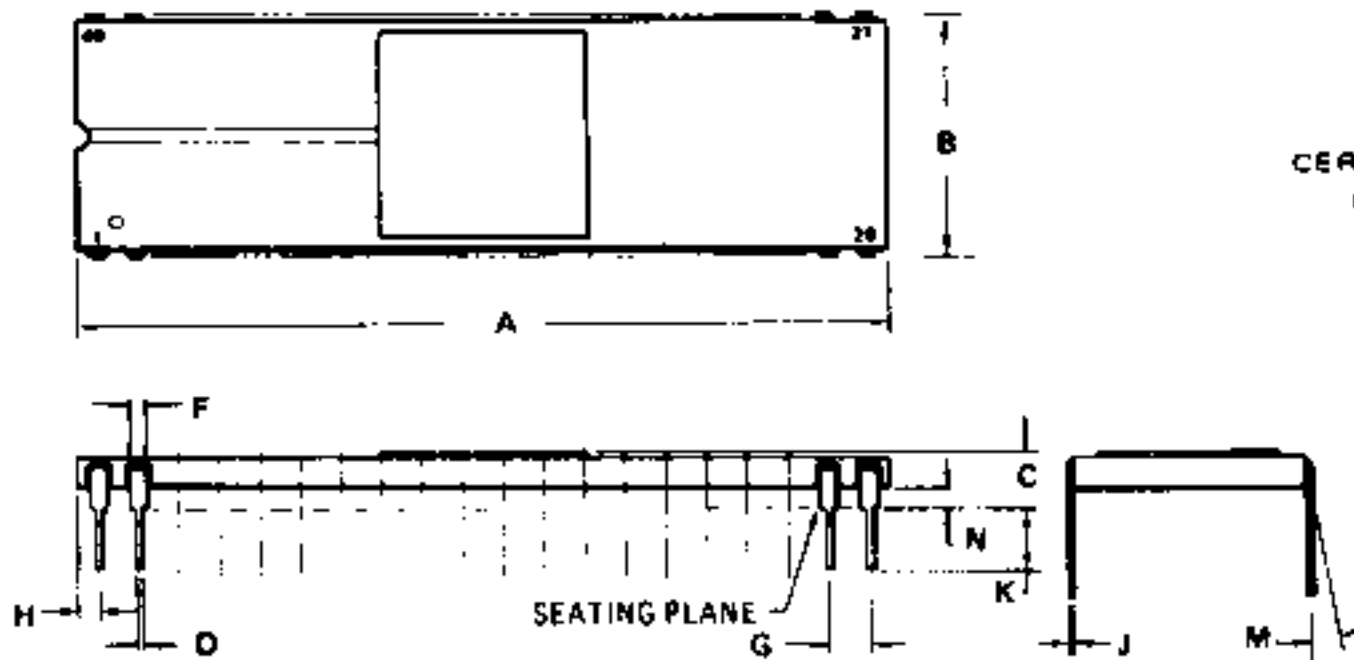
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

NOTE.
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.