8 bit Load Group

Mnemonic	Symbolic Operation	Flags S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	T States	Comments
LD r, r'	r ← r'	•	•	•	•	•	•	•	•	01 r r'		1	1	4	4	r, r' Reg.
LD p, p'*	p ← p'	•	•	•	•	•	•	•	•	11 011 101 01 p p'	DD	2	2	8	4,4	000 B 001 C
LD q, q'*	q ← q'	•	•	•	•	•	•	•	•	11 111 101 01 q q'	FD	2	2	8	4,3	010 D 011 E
LD r, n	r ← n	•	•	•	•	•	•	•	•	00 r 110 ← n →		2	2	7	4,3	100 H 101 L
LD p, n*	p ← n	•	•	•	•	•	•	•	•	11 011 101 00 p 110 ← n →	DD	3	3	11	4,3,3	111 A p, p' Reg.
LD q, n*	q ← n	•	•	•	•	•	•	•	•	11 111 101 00 q 110 ← n →	FD	3	3	11	4,3,3	000 B 001 C 010 D
LD r, (HL)	r ← (HL)	•	•	•	•	•	•	•	•	01 r 110		1	2	7	4,3	011 E
LD r, (IX + d)	r ← (IX + d)	•	•	•	•	•	•	•	•	11 011 101 01 r 110 ← d →	DD	3	5	19	4,4,3,5,3	100 IX_H 101 IX_L 111 A
LD r, (IY + d)	r ← (IY + d)	•	•	•	•	•	•	•	•	11 111 101 01 r 110 ← d →	FD	3	5	19	4,4,3,5,3	 q, q' Reg.
LD (HL), r	(HL) ← r	•	•	•	•	•	•	•	•	01 110 r		1	2	7	4,3	000 B 001 C
LD (IX + d), r	(IX + d) ← r	•	•	•	•	•	•	•	•	11 011 101 01 110 r ← d →	DD	3	5	19	4,4,3,5,3	010 D 011 E 100 IY_H
LD (IY + d), r	(IY + d) ← r	•	•	•	•	•	•	•	•	11 111 101 01 110 r ← d →	FD	3	5	19	4,4,3,5,3	101 IY_L 111 A
LD (HL), n	(HL) ← n	•	•	•	•	•	•	•	•	00 110 110 ← n →	36	2	3	10	4,3,3	
LD (IX + d), n	(IX + d) ← n	•	•	•	•	•	•	•	•	11 011 101 00 110 110 ← d → ← n →	DD 36	4	5	19	4,4,3,5,3	
LD (IY + d), n	(IY + d) ← n	•	•	•	•	•	•	•	•	11 111 101 00 110 110 ← d → ← n →	FD 36	4	5	19	4,4,3,5,3	
LD A, (BC)	A ← (BC)	•	•	•	•	•	•	•	•	00 001 010	0A	1	2	7	4,3	
LD A, (DE)	A ← (DE)	•	•	•	•	•	•	•	•	00 011 010	1A	1	2	7	4,3	
LD A, (nn)	A ← (nn)	•	•	•	•	•	•	•	•	00 111 010 ← n → ← n →	3A	3	4	13	4,3,3,3	
LD (BC), A	(BC) ← A	•	•	•	•	•	•	•	•	00 000 010	02	1	2	7	4,3	
LD (DE), A	(DE) ← A	•	•	•	•	•	•	•	•	00 010 010	12	1	2	7	4,3	
LD (nn), A	(nn) ← A	•	•	•	•	•	•	•	•	00 110 010 ← n → ← n →	32	3	4	13	4,3,3,3	
LD A, I	A ← I	↕	↕	↕	0	↕	IFF_2	0	•	11 101 101 01 010 111	ED 57	2	2	9	4,5	
LD A, R	A ← R	↕	↕	↕	0	↕	IFF_2	0	•	11 101 101 01 011 111	ED 5F	2	2	9	4,5	R is read after it is increased.

LD I, A	I ← A	•	•	•	•	•	•	•	•	11 101 101 01 000 111	ED 47	2	2	9	4,5	
LD R, A	R ← A	•	•	•	•	•	•	•	•	11 101 101 01 001 111	ED 4F	2	2	9	4,5	R is written after it is increased.

Notes: r, r' means any of the registers A, B, C, D, E, H, L.
p, p' means any of the registers A, B, C, D, E, IX_H, IX_L.
q, q' means any of the registers A, B, C, D, E, IY_H, IY_L.
dd_L, dd_H refer to high order and low order eight bits of the register respectively..

Flag Notation: ↕ = flag is set according to the result of the operation, IFF_2 = the interrupt flip-flop 2 is copied.

16 bit Load Group

Mnemonic	Symbolic Operation	S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	T States	Comments
LD dd, nn	dd ← nn	•	•	•	•	•	•	•	•	00 dd0 001 ← n → ← n →		3	3	10	4,3,3	dd Pair 00 BC 01 DE
LD IX, nn	IX ← nn	•	•	•	•	•	•	•	•	11 011 101 00 110 001 ← n → ← n →	DD 21	4	4	14	4,4,3,3	10 HL 11 SP
LD IY, nn	IY ← nn	•	•	•	•	•	•	•	•	11 111 101 00 110 001 ← n → ← n →	FD 21	4	4	14	4,4,3,3	
LD HL, (nn)	L ← (nn) H ← (nn+1)	•	•	•	•	•	•	•	•	00 101 010 ← n → ← n →	2A	3	5	16	4,3,3,3,3	
LD dd, (nn)	dd_L ← (nn) dd_H ← (nn+1)	•	•	•	•	•	•	•	•	11 101 101 01 dd1 011 ← n → ← n →	ED	4	6	20	4,4,3,3,3,3	
LD IX, (nn)	IX_L ← (nn) IX_H ← (nn+1)	•	•	•	•	•	•	•	•	11 011 101 00 101 010 ← n → ← n →	DD 2A	4	6	20	4,4,3,3,3,3	
LD IY, (nn)	IY_L ← (nn) IY_H ← (nn+1)	•	•	•	•	•	•	•	•	11 111 101 00 101 010 ← n → ← n →	FD 2A	4	6	20	4,4,3,3,3,3	
LD (nn), HL	(nn) ← L (nn+1) ← H	•	•	•	•	•	•	•	•	00 100 010 ← n → ← n →	22	3	5	16	4,3,3,3,3	
LD (nn), dd	(nn) ← dd_L (nn+1) ← dd_H	•	•	•	•	•	•	•	•	11 101 101 01 dd0 011 ← n → ← n →	DD	4	6	20	4,4,3,3,3,3	
LD (nn), IX	(nn) ← IX_L (nn+1) ← IX_H	•	•	•	•	•	•	•	•	11 011 101 00 100 010 ← n → ← n →	DD 22	4	6	20	4,4,3,3,3,3	
LD (nn), IY	(nn) ← IY_L (nn+1) ← IY_H	•	•	•	•	•	•	•	•	11 111 101 00 100 010 ← n → ← n →	FD 22	4	6	20	4,4,3,3,3,3	
LD SP, HL	SP ← HL	•	•	•	•	•	•	•	•	11 111 001	F9	1	1	6	6	

LD SP, IX	SP ← IX	•	•	•	•	•	•	•	•	11 011 101 11 111 001	DD F9	2	2	10	4,6		
LD SP, IY	SP ← IY	•	•	•	•	•	•	•	•	11 111 101 11 111 001	FD F9	2	2	10	4,6		
PUSH qq	SP ← SP - 1 (SP) ← qq_H SP ← SP - 1 (SP) ← qq_L	•	•	•	•	•	•	•	•	11 qq0 101		1	3	11	5,3,3	qq 00 01 10 11	Pair BC DE HL AF
PUSH IX	SP ← SP - 1 (SP) ← IX_H SP ← SP - 1 (SP) ← IX_L	•	•	•	•	•	•	•	•	11 011 101 11 100 101	DD E5	2	4	15	4,5,3,3		
PUSH IY	SP ← SP - 1 (SP) ← IY_H SP ← SP - 1 (SP) ← IY_L	•	•	•	•	•	•	•	•	11 111 101 11 100 101	FD E5	2	4	15	4,5,3,3		
POP qq	(SP) ← qq_L SP ← SP + 1 (SP) ← qq_H SP ← SP + 1	•	•	•	•	•	•	•	•	11 qq0 001		1	3	10	4,3,3		
POP IX	(SP) ← IX_L SP ← SP + 1 (SP) ← IX_H SP ← SP + 1	•	•	•	•	•	•	•	•	11 011 101 11 100 001	DD E1	2	4	14	4,4,3,3		
POP IY	(SP) ← IY_L SP ← SP + 1 (SP) ← IY_H SP ← SP + 1	•	•	•	•	•	•	•	•	11 111 101 11 100 001	FD E1	2	4	14	4,4,3,3		

Notes: dd is any of the register pair BC, DE, HL, SP.
qq is any of the register pair BC, DE, HL, AF.

Flag Notation: • = flag is not affected, 0 = flag is reset, 1 = flag is set, ↕ = flag is set according to the result of the operation.

Exchange, Block Transfer and Search Groups

Mnemonic	Symbolic Operation	Flags S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	T States	Comments
EX DE, HL	DE ↔ HL	•	•	•	•	•	•	•	•	11 101 011	EB	1	1	4	4	
EX AF, AF'	AF ↔ AF'	•	•	•	•	•	•	•	•	00 001 000	08	1	1	4	4	
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	•	•	•	•	•	•	•	•	11 011 001	D9	1	1	4	4	
EX (SP), HL	(SP+1) ↔ H (SP) ↔ L	•	•	•	•	•	•	•	•	11 100 011	E3	1	5	19	4,3,4,3,5	
EX (SP), IX	(SP+1) ↔ IX_H (SP) ↔ IX_L	•	•	•	•	•	•	•	•	11 011 101 11 100 011	DD E3	2	6	23	4,4,3,4,3,5	
EX (SP), IY	(SP+1) ↔ IY_H (SP) ↔ IY_L	•	•	•	•	•	•	•	•	11 111 101 11 100 011	FD E3	2	6	23	4,4,3,4,3,5	
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC - 1	•	•	↕[1]	0	↕[2]	↕[3]	0	•	11 101 101 10 100 000	ED A0	2	4	16	4,4,3,5	
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC – 1	•	•	↕[1]	0	↕[2]	0	0	•	11 101 101 10 110 000 Repeat until BC=0	ED B0	2 2	5 4	21 16	4,4,3,5,5 4,4,3,5	if BC ≠ 0 if BC = 0
LDD	(DE) ← (HL) DE ← DE - 1 HL ← HL - 1 BC ← BC – 1	•	•	↕[1]	0	↕[2]	↕[3]	0	•	11 101 101 10 101 000	ED A8	2	4	16	4,4,3,5	
LDDR	(DE) ← (HL) DE ← DE - 1 HL ← HL - 1 BC ← BC – 1	•	•	↕[1]	0	↕[2]	0	0	•	11 101 101 10 111 000 Repeat until BC=0	ED B8	2 2	5 4	21 16	4,4,3,5,5 4,4,3,5	if BC ≠ 0 if BC = 0
CPI	A - (HL) HL ← HL + 1 BC ← BC -1	↕[4]	↕[4]	↕[5]	↕[4]	↕[6]	↕[3]	1	•	11 101 101 10 100 001	ED A1	2	4	16	4,4,3,5	
CPIR	A - (HL) HL ← HL + 1 BC ← BC -1 Repeat until: A = (HL) or BC = 0	↕[4]	↕[4]	↕[5]	↕[4]	↕[6]	↕[3]	1	•	11 101 101 10 110 001	ED B1	2 2	5 4	21 16	4,4,3,5,5 4,4,3,5	if BC ≠ 0 and A ≠ (HL). if BC = 0 or A = (HL)
CPD	A - (HL) HL ← HL - 1 BC ← BC -1	↕[4]	↕[4]	↕[5]	↕[4]	↕[6]	↕[3]	1	•	11 101 101 10 101 001	ED A9	2	4	16	4,4,3,5	
CPDR	A - (HL) HL ← HL - 1 BC ← BC -1 Repeat until: A = (HL) or BC = 0	↕[4]	↕[4]	↕[5]	↕[4]	↕[6]	↕[3]	1	•	11 101 101 10 111 001	ED B9	2 2	5 4	21 16	4,4,3,5,5 4,4,3,5	if BC ≠ 0 and A ≠ (HL). if BC = 0 or A = (HL)

Notes:

[1] YF is a copy of bit 1 of A + last transferred byte, thus $(A + (HL))_1$

[2] XF is a copy of bit 3 of A + last transferred byte, thus $(A + (HL))_3$

[3] P/V flag is 0 if the result of BC - 1 = 0, otherwise P/V = 1.

[4] These flags are set as in CP (HL)

[5] YF is copy of bit 1 of A - last compared address - H, thus $(A - (HL) - H)_1$. H is as in F after the comparison.

[6] XF is copy of bit 3 of A - last compared address - H, thus $(A - (HL) - H)_3$. H is as in F after the comparison.

Flag Notation: • = flag is not affected, 0 = flag is reset, 1 = flag is set, ↕ = flag is set according to the result of the operation.

8 bit Arithmetic and Logical Group

Mnemonic	Symbolic Operation	Flags S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	T States	Comments
ADD A, r	A ← A + r	↕	↕	↕	↕	↕	V	0	↕	10 000 r		1	1	4	4	r Reg. p Reg.
ADD A, p*	A ← A + p	↕	↕	↕	↕	↕	V	0	↕	11 011 101 10 000 p	DD	2	2	8	4,4	000 B 000 B 001 C 001 C
ADD A, q*	A ← A + q	↕	↕	↕	↕	↕	V	0	↕	11 111 101 10 000 q	FD	2	2	8	4,4	010 D 010 D 011 E 011 E
ADD A, n	A ← A + n	↕	↕	↕	↕	↕	V	0	↕	11 000 110 ← n →		2	2	7	4,3	100 H 100 IX_H 101 L 101 IX_L
ADD A, (HL)	A ← A + (HL)	↕	↕	↕	↕	↕	V	0	↕	10 000 110		1	2	7	4,3	111 A 111 A
ADD A, (IX + d)	A ← A + (IX + d)	↕	↕	↕	↕	↕	V	0	↕	11 011 101 10 000 110 ← d →	DD	3	5	19	4,4,3,5,3	
ADD A, (IY + d)	A ← A + (IY + d)	↕	↕	↕	↕	↕	V	0	↕	11 111 101 10 000 110 ← d →	FD	3	5	19	4,4,3,5,3	
ADC A, s	A ← A + s + CY	↕	↕	↕	↕	↕	V	0	↕	001						s is any of r, n, (HL), (IX+d), (IY+d), p, q as shown for the ADD instruction. The underlined bits replace the underlined bits in the ADD set.
SUB A, s	A ← A - s	↕	↕	↕	↕	↕	V	1	↕	010						
SBC A, s	A ← A - s - CY	↕	↕	↕	↕	↕	V	1	↕	011						
AND s	A ← A AND s	↕	↕	↕	1	↕	P	0	0	100						
OR s	A ← A OR s	↕	↕	↕	0	↕	P	0	0	110						
XOR s	A ← A XOR s	↕	↕	↕	0	↕	P	0	0	101						
CP s	A - s	↕	↕	↕[1]	↕	↕[1]	V	1	↕	111						
INC r	r ← r + 1	↕	↕	↕	↕	↕	V	0	•	00 r 100		1	1	4	4	
INC p*	p ← p + 1	↕	↕	↕	↕	↕	V	0	•	11 011 101 00 p 100	DD	2	2	8	4,4	q Reg. 000 B
INC q*	q ← q + 1	↕	↕	↕	↕	↕	V	0	•	11 111 101 00 q 100	FD	2	2	8	4,4	001 C 010 D
INC (HL)	(HL) ← (HL) + 1	↕	↕	↕	↕	↕	V	0	•	00 110 100		1	3	11	4,4,3	011 E
INC (IX + d)	(IX + d) ← (IX + d) + 1	↕	↕	↕	↕	↕	V	0	•	11 011 101 00 110 100 ← d →	DD	3	6	23	4,4,3,5,4,3	100 IY_H 101 IY_L 111 A
INC (IY + d)	(IY + d) ← (IY + d) + 1	↕	↕	↕	↕	↕	V	0	•	11 111 101 00 110 100 ← d →	FD	3	6	23	4,4,3,5,4,3	
DEC m	m ← m - 1	↕	↕	↕	↕	↕	V	1	•	101						m is any of r, p, q, (HL), (IX+d), (IY+d), as shown for the INC instruction. DEC same format and states as INC. Replace 100 with 101 in opcode.

Notes:

[1] XF and YF are copied from the operand (s), not from the result of (A - s).

The V symbol in the P/V flag column indicates that the P/V flags contains the overflow of the operation. Similarly the P symbol indicates parity.

Flag Notation:

• = flag is not affected, 0 = flag is reset, 1 = flag is set, ↕ = flag is set according to the result of the operation.

16 bit Arithmetic Group

Mnemonic	Symbolic Operation	Flags S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	T States	Comments
ADD HL, ss	HL ← HL + ss	•	•	↕[2]	↕[2]	↕[2]	•	0	↕[1]	00 ss1 001		1	3	11	4,4,3	ss Reg.
ADC HL, ss	HL ← HL + ss + CY	↕[1]	↕[1]	↕[2]	↕[2]	↕[2]	V[1]	0	↕[1]	11 101 101	ED	2	4	15	4,4,4,3	00 BC
										01 ss1 010						01 DE
SBC HL, ss	HL ← HL - ss - CY	↕[1]	↕[1]	↕[2]	↕[2]	↕[2]	V[1]	1	↕[1]	11 101 101	ED	2	4	15	4,4,4,3	10 HL
										01 ss0 010						11 SP
ADD IX, pp	IX ← IX + pp	•	•	↕[2]	↕[2]	↕[2]	•	0	↕[1]	11 011 101	DD	2	4	15	4,4,4,3	
										00 pp1 001						pp Reg.
ADD IY, rr	IY ← IY + rr	•	•	↕[2]	↕[2]	↕[2]	•	0	↕[1]	11 111 101	FD	2	4	15	4,4,4,3	00 BC
										00 rr1 001						01 DE
INC ss	ss ← ss + 1	•	•	•	•	•	•	•	•	00 ss0 011		1	1	6	6	10 IX
INC IX	IX ← IX + 1	•	•	•	•	•	•	•	•	11 011 101	DD	2	2	10		11 SP
										00 100 011	23					
INC IY	IY ← IY + 1	•	•	•	•	•	•	•	•	11 111 101	FD	2	2	10	4,6	rr Reg.
										00 100 011	23					00 BC
DEC ss	ss ← ss - 1	•	•	•	•	•	•	•	•	00 ss1 011		1	1	6	6	01 DE
DEC IX	IX ← IX - 1	•	•	•	•	•	•	•	•	11 011 101	DD	2	2	10	4,6	10 IY
										00 101 011	2B					11 SP
DEC IY	IY ← IY - 1	•	•	•	•	•	•	•	•	11 111 101	FD	2	2	10	4,6	
										00 101 011	2B					

Notes:
16 bit additions are performed by first adding the two low order eight bits, and then the two high order eight bits.
[1] Indicates the flag is affected by the 16 bit result of the operation.
[2] Indicates the flag is affected by the 8 bit addition of the high order eight bits

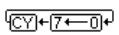
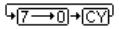
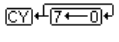
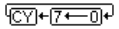
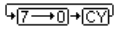
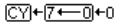
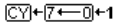
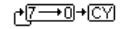
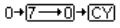
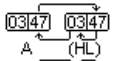
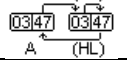
General Purpose Arithmetic and CPU Control Groups

Mnemonic	Symbolic Operation	Flags S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	T States	Comments
DAA	Adjust A	↕	↕	↕[1]	↕	↕[1]	P	•	↕	00 100 111	27	1	1	4	4	
CPL	$A \leftarrow \overline{A}$	•	•	↕[1]	1	↕[1]	•	1	•	00 101 111	2F	1	1	4	4	One's complement.
NEG[4]	A ← 0 - A	↕	↕	↕[1]	↕	↕[1]	V	1	↕	11 101 101	ED	2	2	8	4,4	Two's complement.
										01 000 100	44					
CCF	$CY \leftarrow \overline{CY}$	•	•	↕[1]	↕[2]	↕[1]	•	0	↕	00 111 111	3F	1	1	4	4	Complement carry flag.
SCF	CY ← 1	•	•	↕[1]	0	↕[1]	•	0	1	00 110 111	37	1	1	4	4	
NOP	No operations	•	•	•	•	•	•	•	•	00 000 000	00	1	1	4	4	
HALT	CPU halted	•	•	•	•	•	•	•	•	01 110 110	76	1	1	4	4	
DI[3]	$IFF_1 \leftarrow 0$	•	•	•	•	•	•	•	•	11 110 011	F3	1	1	4	4	
	$IFF_2 \leftarrow 0$															
EI[3]	$IFF_1 \leftarrow 1$	•	•	•	•	•	•	•	•	11 111 011	FB	1	1	4	4	
	$IFF_2 \leftarrow 1$															
IM 0[4]	Set interrupt mode 0	•	•	•	•	•	•	•	•	11 101 101	ED	2	2	8	4,4	
										01 000 110	46					
IM 1[4]	Set interrupt mode 1	•	•	•	•	•	•	•	•	11 101 101	ED	2	2	8	4,4	
										01 010 110	56					
IM 2[4]	Set interrupt mode 2	•	•	•	•	•	•	•	•	11 101 101	ED	2	2	8	4,4	
										01 011 110	5E					

Notes:
[1] XF and YF are a copy of bit 5 and 3 of register A
[2] H contains the previous carry state (after instruction $H \leftrightarrow C$)
[3] No interrupts are issued directly after a DI or EI.
[4] This instruction has other unofficial opcodes, see Opcodes list.

Flag Notation:
• = flag is not affected, 0 = flag is reset, 1 = flag is set, ↕ = flag is set according to the result of the operation.

Rotate and Shift Group

Mnemonic	Symbolic Operation	S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	T States	Comments
RLCA		•	•	↕	0	↕	•	0	↕	00 000 111	07	1	1	4	4	
RLA		•	•	↕	0	↕	•	0	↕	00 010 111	17	1	1	4	4	
RRCA		•	•	↕	0	↕	•	0	↕	00 001 111	0F	1	1	4	4	
RRA		•	•	↕	0	↕	•	0	↕	00 011 111	1F	1	1	4	4	
RLC r		↕	↕	↕	0	↕	P	0	↕	11 001 011 00 000 r	CB	2	2	8	4,4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLC (HL)		↕	↕	↕	0	↕	P	0	↕	11 001 011 00 000 110	CB	2	4	15	4,4,4,3	
RLC (IX + d)		↕	↕	↕	0	↕	P	0	↕	11 011 101 11 001 011 ← d → 00 000 110	DD CB	4	6	23	4,4,3,5,4,3	
RLC (IY + d)		↕	↕	↕	0	↕	P	0	↕	11 111 101 11 001 011 ← d → 00 000 110	FD CB	4	6	23	4,4,3,5,4,3	
LD r,RLC (IX + d)*	r ← (IX + d) RLC r (IX + d) ← r	↕	↕	↕	0	↕	P	0	↕	11 011 101 11 001 011 ← d → 00 000 r	DD CB	4	6	23	4,4,3,5,4,3	
LD r,RLC (IY + d)*	r ← (IY + d) RLC r (IY + d) ← r	↕	↕	↕	0	↕	P	0	↕	11 111 101 11 001 011 ← d → 00 000 r	FD CB	4	6	23	4,4,3,5,4,3	
RL m		↕	↕	↕	0	↕	P	0	↕	010						Instruction format
RRC m		↕	↕	↕	0	↕	P	0	↕	001						and states are the
RR m		↕	↕	↕	0	↕	P	0	↕	011						same as RLC.
SLA m		↕	↕	↕	0	↕	P	0	↕	100						Replace 000 with
SLL m*		↕	↕	↕	0	↕	P	0	↕	110						new number.
SRA m		↕	↕	↕	0	↕	P	0	↕	101						
SRL m		↕	↕	↕	0	↕	P	0	↕	111						
RLD		↕	↕	↕	0	↕	P	0	•	11 101 101 01 101 111	ED 6F	2	5	18	4,4,3,4,3	
RRD		↕	↕	↕	0	↕	P	0	•	11 101 101 01 100 111	ED 67	2	5	18	4,4,3,4,3	

Notes: The P symbol in the P/V flag column indicates that the P/V flags contains the parity of the result.

Flag Notation: • = flag is not affected, 0 = flag is reset, 1 = flag is set, ↕ = flag is set according to the result of the operation.

Bit Manipulation Group

Mnemonic	Symbolic Operation	Flags S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	T States	Comments
BIT b, r	$Z \leftarrow \overline{r_b}$	↕[1]	↕	↕[2]	1	↕[3]	↕[4]	0	•	11 001 011 01 b r	CB	2	2	8	4,4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
BIT b, (HL)	$Z \leftarrow \overline{(HL)_b}$	↕[1]	↕	↕[2]	1	↕[3]	↕[4]	0	•	11 001 011 01 b 110	CB	2	3	12	4,4,4	
BIT b, (IX + d)[5]	$Z \leftarrow \overline{(IX + d)_b}$	↕[1]	↕	↕[2]	1	↕[3]	↕[4]	0	•	11 011 101 11 001 011 ← d → 01 b 110	DD CB	4	5	20	4,4,3,5,4	
BIT b, (IY + d)[5]	$Z \leftarrow \overline{(IY + d)_b}$	↕[1]	↕	↕[2]	1	↕[3]	↕[4]	0	•	11 111 101 11 001 011 ← d → 01 b 110	FD CB	4	5	20	4,4,3,5,4	
SET b, r	$r_b \leftarrow 1$	•	•	•	•	•	•	•	•	11 001 011 11 b r	CB	2	2	8	4,4	b Bit. 000 0 001 1 010 2 011 3 100 4 101 5 110 6 111 7
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	•	•	•	•	•	•	11 001 011 11 b 110	CB	2	4	15	4,4,4,3	
SET b, (IX + d)	$(IX + d)_b \leftarrow 1$	•	•	•	•	•	•	•	•	11 011 101 11 001 011 ← d → 11 b 110	DD CB	4	6	23	4,4,3,5,4,3	
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	•	•	•	•	•	•	•	•	11 111 101 11 001 011 ← d → 11 b 110	FD CB	4	6	23	4,4,3,5,4,3	
LD r,SET b, (IX + d)*	$r \leftarrow (IX + d)$ $r_b \leftarrow 1$ $(IX + d) \leftarrow r$	•	•	•	•	•	•	•	•	11 011 101 11 001 011 ← d → 11 b r	DD CB	4	6	23	4,4,3,5,4,3	
LD r,SET b, (IY + d)*	$r \leftarrow (IY + d)$ $r_b \leftarrow 1$ $(IY + d) \leftarrow r$	•	•	•	•	•	•	•	•	11 111 101 11 001 011 ← d → 11 b r	FD CB	4	6	23	4,4,3,5,4,3	
RES b, m	$m_b \leftarrow 0$ m ≡ r, (HL), (IX+d), (IY+d)	•	•	•	•	•	•	•	•	10						To form new opcode replace 11 of SET b, s with 10. Flags and states are the same.

Notes:

The notation m_b indicates bit b (0 to 7) of location m.
BIT instructions are performed by an bitwise AND.
[1] S is set if b = 7 and Z = 0
[2] YF is set if b = 5 and Z = 0
[3] XF is set if b = 3 and Z = 0
[4] P/V is set like the Z flag
[5] This instruction has other unofficial opcodes

Flag Notation: • = flag is not affected, 0 = flag is reset, 1 = flag is set, ↕ = flag is set according to the result of the operation.

Input and Output Groups

Mnemonic	Symbolic Operation	Flags S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	T States	Comments
IN A, (n)	A ← (n)	•	•	•	•	•	•	•	•	11 011 011 ← n →	DB	2	3	11	4,3,4	r Reg. 000 B
IN r, (C)	r ← (C)	↕	↕	↕	0	↕	P	0	•	11 101 101 01 r 000	ED	2	3	12	4,4,4	001 C 010 D
IN (C)* or IN F, (C)*	Just affects flags, value is lost.	↕	↕	↕	0	↕	P	0	•	11 101 101 01 110 000	ED 70	2	3	12	4,4,4	011 E 100 H
INI	(HL) ← (C) HL ← HL + 1 B ← B - 1	↕[1]	↕[1]	↕[1]	↕[3]	↕[1]	↕[3]	↕[2]	↕[3]	11 101 101 10 100 010	ED A2	2	4	16	4,5,4,3	101 L 111 A
INIR	(HL) ← (C) HL ← HL + 1 B ← B - 1 Repeat until B = 0	0	1	0	↕[3]	0	↕[3]	↕[2]	↕[3]	11 101 101 10 110 010	ED B2	2 2	5 4	21 16	4,5,4,3,5 4,5,4,3	if B ≠ 0 if B = 0
IND	(HL) ← (C) HL ← HL - 1 B ← B - 1	↕[1]	↕[1]	↕[1]	↕[4]	↕[1]	↕[3]	↕[2]	↕[4]	11 101 101 10 101 010	ED AA	2	4	16	4,5,4,3	
INDR	(HL) ← (C) HL ← HL - 1 B ← B - 1 Repeat until B = 0	0	1	0	↕[4]	0	↕[3]	↕[2]	↕[4]	11 101 101 10 111 010	ED BA	2 2	5 4	21 16	4,5,4,3,5 4,5,4,3	if B ≠ 0 if B = 0
OUT (n), A	(n) ← A	•	•	•	•	•	•	•	•	11 010 011 ← n →	D3	2	3	11	4,3,4	
OUT (C), r	(C) ← r	•	•	•	•	•	•	•	•	11 101 101 01 r 001	ED	2	3	12	4,4,4	
OUT (C), 0*	(C) ← 0	•	•	•	•	•	•	•	•	11 101 101 01 110 001	ED 71	2	3	12	4,4,4	
OUTI	(C) ← (HL) HL ← HL + 1 B ← B - 1	↕[1]	↕[1]	↕[1]	↕[3]	↕[1]	↕[3]	↕[2]	↕[3]	11 101 101 10 100 011	ED A3	2	4	16	4,5,4,3	
OTIR	(C) ← (HL) HL ← HL + 1 B ← B - 1 Repeat until B = 0	0	1	0	↕[3]	0	↕[3]	↕[2]	↕[3]	11 101 101 10 110 011	ED B3	2 2	5 4	21 16	4,5,4,3,5 4,5,4,3	if B ≠ 0 if B = 0
OUTD	(C) ← (HL) HL ← HL - 1 B ← B - 1	↕[1]	↕[1]	↕[1]	↕[3]	↕[1]	↕[3]	↕[2]	↕[3]	11 101 101 10 101 011	ED AB	2	4	16	4,5,4,3	
OTDR	(C) ← (HL) HL ← HL - 1 B ← B - 1 Repeat until B = 0	0	1	0	↕[3]	0	↕[3]	↕[2]	↕[3]	11 101 101 10 111 011	ED BB	2 2	5 4	21 16	4,5,4,3,5 4,5,4,3	if B ≠ 0 if B = 0

Notes:

The V symbol in the P/V flag column indicates that the P/V flags contains the overflow of the operation. Similarly the P symbol indicates parity.

r means any of the registers A, B, C, D, E, H, L.

[1] flag is affected by the result of B ← B - 1 as in DEC B.

[2] N is a copy bit 7 of the last value from the input (C).

[3] This flag is bizarre, see section 4.3.

Jump Group

Mnemonic	Symbolic Operation	S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	T States	Comments
JP nn	PC ← nn	•	•	•	•	•	•	•	•	11 000 011 ← n → ← n →	C3	3	3	10	4,3,3	
JP cc, nn	if cc is true, PC ← nn	•	•	•	•	•	•	•	•	11 ccc 010 ← n → ← n →		3	3	10	4,3,3	ccc Condition 000 NZ 001 Z 010 NC 011 C 100 PO 101 PE 110 P 111 M
JR e	PC ← PC + e	•	•	•	•	•	•	•	•	00 011 000 ← e - 2 →	18	2	3	12	4,3,5	
JR ss, e	if ss is true PC ← PC + e	•	•	•	•	•	•	•	•	00 1ss 000 ← e - 2 →		2 2	3 2	12 7	4,3,5 4,3	if ss is true if ss is false
JP HL	PC ← HL	•	•	•	•	•	•	•	•	11 101 001	E9	1	1	4	4	
JP IX	PC ← IX	•	•	•	•	•	•	•	•	11 011 101 11 101 001	DD E9	2	2	8	4,4	ss Condition 11 C 10 NC 01 Z 00 NZ
JP IY	PC ← IY	•	•	•	•	•	•	•	•	11 111 101 11 101 001	FD E9	2	2	8	4,4	
DJNZ e	B ← B - 1 if B ≠ 0 PC ← PC + e	•	•	•	•	•	•	•	•	00 010 000 ← e - 2 →	10	2 2	2 3	8 13	5,3 5,3,5	if B = 0 if B ≠ 0

Notes:
e is a signed two-complement number in the range <-126, 129>
e - 2 in the opcode provides an effective number of PC + e as PC incremented by 2 prior to the addition of e.
ccc is a 3-bit condition
ss is a 2-bit condition

Flag Notation:
• = flag is not affected, 0 = flag is reset, 1 = flag is set, ↕ = flag is set according to the result of the operation.

Call and Return Group

Mnemonic	Symbolic Operation	S	Z	YF	H	XF	P/V	N	C	Opcode 76 543 210	Hex	No.of Bytes	No.of M Cycles	No.of T States	T States	Comments
CALL nn	SP ← SP - 1 (SP) ← PC_H SP ← SP - 1 (SP) ← PC_L PC ← nn	•	•	•	•	•	•	•	•	11 001 101 ← n → ← n →	CD	3	5	17	4,3,4,3,3	
CALL cc, nn	if cc is true, SP ← SP - 1 (SP) ← PC_H SP ← SP - 1 (SP) ← PC_L PC ← nn	•	•	•	•	•	•	•	•	11 ccc 100 ← n → ← n →		3 3	3 5	10 17	4,3,3 4,3,4,3,3	if cc is false if cc is true
RET	PC_L ← (SP) SP ← SP + 1 PC_H ← (SP) SP ← SP + 1	•	•	•	•	•	•	•	•	11 001 001	C9	1	3	10	4,3,3	
RET cc	if cc is true, PC_L ← (SP) SP ← SP + 1 PC_H ← (SP) SP ← SP + 1	•	•	•	•	•	•	•	•	11 ccc 000		1 1	1 3	5 11	5 5,3,3	if cc is false if cc is true
RETI[2]	PC_L ← (SP) SP ← SP + 1 PC_H ← (SP) SP ← SP + 1	•	•	•	•	•	•	•	•	11 101 101 01 001 101	ED 4D	2	4	14	4,4,3,3	ccc Condition 000 NZ 001 Z 010 NC 011 C
RETN[1,2]	PC_L ← (SP) SP ← SP + 1 PC_H ← (SP) SP ← SP + 1 IFF_1 ← IFF_2	•	•	•	•	•	•	•	•	11 101 101 01 000 101	ED 45	2	4	14	4,4,3,3	100 PO 101 PE 110 P 111 M
RST p	SP ← SP - 1 (SP) ← PC_H SP ← SP - 1 (SP) ← PC_L PC ← p	•	•	•	•	•	•	•	•	11 t 111		1	3	11	5,3,3	t p 000 0h 001 8h 010 10h 011 18h 100 20h 101 28h 110 30h 111 38h

Notes:
[1] This instruction has other unofficial opcodes, see Opcode list. RETI and RETN are internally the same instruction.
[2] Instruction also IFF_1 ← IFF_2
cc is a 3-bit condition

Flag Notation:
• = flag is not affected, 0 = flag is reset, 1 = flag is set, ↕ = flag is set according to the result of the operation.