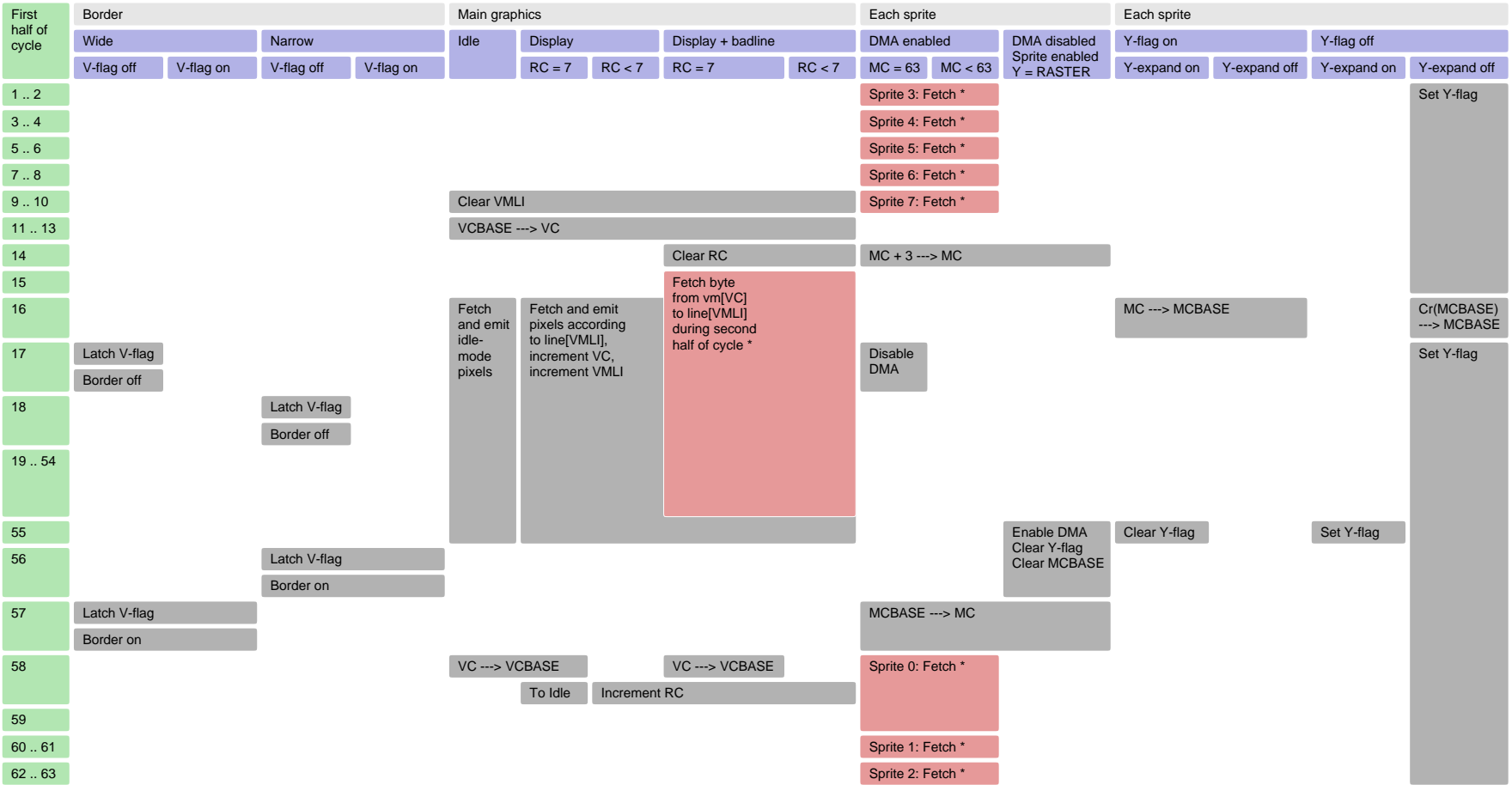


VIC 6569/8565 Timing Chart



* The CPU is stalled on read accesses, starting three cycles before the fetch provided that the fetch could be anticipated.

Every cycle of rasterline	V-flag latch action				Main graphics			
	Tall		Short		DEN on	DEN off	YSCROLL matches	
	D-flag on	D-flag off	D-flag on	D-flag off		At cycle 1	D-flag on	Display + badline
\$00 .. \$2F	Keep	Keep	Keep	Keep	Clear VCBASE			
\$30					Set D-flag	Clear D-flag	To Display + badline	
\$31 .. \$32					To Display			
\$33	Clear							
\$34 .. \$36	Keep							
\$37			Clear					
\$38 .. \$F6			Keep					
\$F7			Set	Set				
\$F8 .. \$FA			Keep	Keep				
\$FB	Set	Set						
\$FC .. \$137	Keep	Keep						

Sprite crunch function, Cr(MCBASE)								
From	To	Deviation	From	To	Deviation	From	To	Deviation
00	01	-2	01	05	1		02	
03	07	1	04	05	-2		05	05 -3
06	05	-4	07	07	-3		08	09 -2
09	0d	1	0A				0b	0f 1
0C	0d	-2	0D	15	5		0e	15 4
0F	17	5	10	11	-2		11	15 1
12			13	17	1		14	15 -2
15	15	-3	16	15	-4		17	17 -3
18	19	-2	19	1d	1		1a	
1B	1f	1	1C	1d	-2		1d	15 -11
1E	15	-12	1F	17	-11		20	21 -2
21	25	1	22				23	27 1
24	25	-2	25	25	-3		26	25 -4
27	27	-3	28	29	-2		29	2d 1
2A			2B	2f	1		2c	2d -2
2D	35	5	2E	35	4		2f	37 5
30	31	-2	31	35	1		32	
33	37	1	34	35	-2		35	35 -3
36	35	-4	37	37	-3		38	39 -2
39	3d	1	3A				3b	3f 1
3C	3d	-2	3D	15	-43		3e	15 -44