Appendix XII
The Hardware.

A. Processor.

The processor is a Z80A running at a clock frequency of 4.00 MHz (±0.1%). There is logic that stretches /MREQ and /IORQ using the CPU WAIT facility so that the processor can only make one access to memory each microsecond.

The processor /NMI pin is pulled up and made available on the expansion bus. However, a non-maskable interrupt may cause the firmware to violate various timing constraints and so its use is not recommended.

The processor interrupt pin is driven by a flip-flop in the video gate array. This flip-flop is set during every vertical flyback and every 52 scan lines thereafter until the next vertical flyback. The interrupt is arranged to occur approximately 2 scans (125 microseconds) into the 8 scan (500 microsecond) vertical flyback signal. The interrupt latch is cleared by the processor acknowledging the interrupt, or explicitly, using a software command. The top bit of the divide by 52 scan counter is also cleared when the processor acknowledges an interrupt occurring after this counter has overflowed. This allows the interrupt system to be expanded.

B. Memory.

ROM

A single 32K byte ROM is present on the processor board, but is mapped onto two blocks of 16K in processor address space. The lower half of the ROM occupies addresses #0000 to #3FFF and the upper half occupies addresses #C000 to #FFFF. These two halves of the ROM can be separately enabled and disabled by two control latches in the video gate array. On power-up or other system reset both halves of the ROM are enabled.

An expansion port signal can be used to disable this internal ROM and allow external ROM(s) to be accessed instead. These are selected by output instructions and replace the upper half of the on-board 32K byte ROM when selected.

RAM

64K bytes of dynamic RAM are fitted to the processor board at addresses #0000 to #FFFF. The lowest 16K and the top 16K are overlayed when ROM is enabled. Whether the ROM is enabled or not affects where data is read from, it has no effect on write operations which will be correctly performed ‘through’ the enabled ROM to the underlying RAM.

VDU SCREEN MEMORY

The display uses 16k of the processor RAM memory as screen refresh memory. The 16k used can be switched between the blocks starting at #0000, #4000, #8000 and at #C000 by the top two bits (bits 12 and 13) programmed into the HD6845S start address register (see section 6.4 for further details).

The arrangement of data in the VDU screen memory is dependent on the VDU mode currently selected. In all modes the memory can be considered as consisting of 8K 16 bit words. Each word contains either 4, 8 or 16 pixels (P0..Pn) of 1, 2 or 4 bits (B0..Bm) depending on the mode as follows:

A0	Bit	Mode 0	Mode 1	Mode 2
0	D7	P0 B0	P0 B0	P0 B0
0	D6	P1 B0	P1 B0	P1 B0
0	D5	P0 B1	P2 B0	P2 B0
0	D4	P1 B1	P3 B0	P3 B0
0	D3	P0 B2	P0 B1	P4 B0
0	D2	P1 B2	P1 B1	P5 B0
0	D1	P0 B3	P2 B1	P6 B0
0	D0	P1 B3	P3 B1	P7 B0
1	D7	P2 B0	P4 B0	P8 B0
1	D6	P3 B0	P5 B0	P9 B0
1	D5	P2 B1	P6 B0	P10 B0
1	D4	P3 B1	P7 B0	P11 B0
1	D3	P2 B2	P4 B1	P12 B0
1	D2	P3 B2	P5 B1	P13 B0
1	D1	P2 B3	P6 B1	P14 B0
1	D0	P3 B3	P7 B1	P15 B0

Data for lines 0,8,16,24.. on the display are packed into the first 2K byte block of the memory, lines 1,9,17,25.. are packed into the corresponding places of the next 2K byte block of memory, with lines 7,15,23,31.. occupying the top 2K byte block of the 16k memory area.

The bottom 10 bits of the HD6845SP start address register define where within these 2K blocks the screen starts. The offset from the start of the 2K byte block is always even and is calculated as twice the register contents modulo 2K bytes. When data has to be displayed from beyond the end of a 2K byte block wrap around occurs to the begining of the same 2K byte block. See section 6.4 for a fuller description.

C. Interfaces.

The standard interfaces on the processor board occupy I/O channels on the Z80 as follows:

I/O Address	Output use	Input use
#7Fxx	Video gate array	** Do not use **
#BCxx	HD6845S CRTC address	** Do not use **
#BDxx	HD6845S CRTC data	** Do not use **
#BExx	** Do not use **	Reserved for CRTC status
#BFxx	** Do not use **	HD6845S CRTC data
#DFxx	Expansion ROM select	** Not used **
#EFxx	Centronics latch	** Do not use **
#F4xx	µPD8255 port A data	µPD8255 port A data
#F5xx	µPD8255 port B data	µPD8255 port B data
#F6xx	µPD8255 port C data	µPD8255 port C data
#F7xx	µPD8255 control	** Undefined **
#F8xx	Expansion bus	Expansion bus
#F9xx	Expansion bus	Expansion bus
#FAxx	Expansion bus	Expansion bus
#FBxx	Expansion bus	Expansion bus
#FFxx	** Not used **	** Not used **

Note that the Z80 instructions that place an address on the top half of the address bus (A8..A15) must be used. Use of block I/O instructions that alter register B during the instruction is not recommended. I/O addresses such as those below #7Fxx that do not occur in the above table should not be used at all.

Expansion bus peripherals must decode addresses on A0..A7 whilst address line A10 is low. (Additionally address lines A8 and A9 may be decoded to select a device or register on the peripheral). Expansion bus I/O channels in the address range #F800 to #FBFF are reserved as follows:

Address (A0..A7)	Use
#00..#7B	** Do not use **
#7C..#7F	Reserved for disc interface.
#80..#BB	** Do not use **
#BC..#BF	Reserved for future use.
#C0..#DB	** Do not use **
#DC..#DF	Reserved for communications interfaces.
#E0..#FE	Available for user peripherals.
#FF	Reset peripherals.

All expansion peripherals should be reset when an output is performed to I/O channel #F8FF. In particular a peripheral that generates interrupts must not generate an interrupt until it is re-initialised after such an output has been performed.

D. AY-3-8912 Programmable Sound Generator.

The PSG is accessed using ports A and C of the µPD8255 device. Note that when writing or loading address to the AY-3-8912 the maximum duration of the write or load address command with BDIR high is 10 microseconds. The clock input to the sound generator is exactly 1.00 MHz. The BC2 signal is tied permanently high. On power-up the I/O port should be programmed to input mode.

The user is advised to use the firmware routine MC SOUND REGISTER to write to the PSG.

e. HD6845S CRT Controller (HD6845S CRTC).

The character clock to the CRTC occurs for every two bytes fetched from memory, i.e. every 1.0 microseconds. The first byte of a pair has an even address, the second has an odd address. In normal operation the internal registers are set up as follows:

Register	Function	PAL	SECAM	NTSC
0	Horizontal Total	63	63	63
1	Horizontal Displayed	40	40	40
2	Horizontal Sync. Posn.	46	46	46
3	Vsync., Hsync. widths	#8E	#8E	#8E
4	Vertical Total	38	38	31
5	Vertical Total Adjust	0	0	6
6	Vertical Displayed	25	25	25
7	Vertical Sync. Posn.	30	30	30
8	Interlace and Skew	0	0	0
9	Max. Raster Address	7	7	7
10	Cursor Start Raster	X	X	X
11	Cursor End Raster	X	X	X
12	Start Address (H)	X	X	X
13	Start Address (L)	X	X	X
14	Cursor (H)	X	X	X
15	Cursor (L)	X	X	X

In the above table the numbers for PAL and SECAM standards are identical.

Note that X indicates that software may vary these numbers during device operation. The firmware only makes use of the start address register which is used to set the screen base and offset.

F. Video Gate Array.

The software must access this device in order to control the enabling and disabling of ROMs, the mode of operation of the VDU and also to load colour information for 'inks' into the palette memory. One I/O channel is used for all commands, the top two bits of data specifying the command type as follows:

Bit 7	Bit 6	Use
0	0	Load palette pointer register.
0	1	Load palette memory.
1	0	Load mode and ROM enable register.
1	1	Reserved.

MODE AND ROM ENABLE REGISTER

This write- only register controls the VDU mode and ROM enabling as follows:

Bit 7:	1
Bit 6:	0
Bit 5:	** Reserved ** (send 0)
Bit 4:	Clear raster 52 divider.
Bit 3:	Upper half ROM disable.
Bit 2:	Lower half ROM disable.
Bit 1:	VDU Mode control MC1.
Bit 0:	VDU Mode control MC0.

Writing a 1 to bit 4 clears the top bit of the divide by 52 counter used for generating periodic interrupts.

Modes are defined by the mode control pins as follows:

MC1	MC0	Mode
0	0	Mode 0, 160 x 200 pixels in 16 colours
0	1	Mode 1, 320 x 200 pixels in 4 colours.
1	0	Mode 2,640 x 200 pixels in 2 colours.
1	1	** Do not use **

The gate array hardware synchronises mode changing to the next horizontal flyback in order to aid software that requires different parts of the screen to be handled in different modes.

On power-up and other system resets, the mode and ROM enable register is set to zero, enabling both halves of the ROM.

PALETTE POINTER REGISTER

This write- only register controls the loading of the VDU colour palette as follows:

Bit 7:	0
Bit 6:	0
Bit 5:	** Reserved ** (send 0)
Bit 4:	Palette pointer bit PR4.
Bit 3:	Palette pointer bit PR3.
Bit 2:	Palette pointer bit PR2.
Bit 1:	Palette pointer bit PR1.
Bit 0:	Palette pointer bit PR0.

Bits PR0 to PR3 select which ink is to have its colour loaded, providing bit PR4 is low. If bit PR4 is high then bits PR0 to PR3 are ignored and the border ink colour is loaded.

PALETTE MEMORY

This write-only memory controls the VDU colour palette as follows:

Bit 7:	0
Bit 6:	1
Bit 5:	** Reserved ** (send 0)
Bit 4:	Colour data bit CD4.
Bit 3:	Colour data bit CD3.
Bit 2:	Colour data bit CD2.
Bit 1:	Colour data bit CD1.
Bit 0:	Colour data bit CD0.

The ink entry pointed at by the palette pointer register is loaded with the colour sent on this channel. The number of colours that need to be loaded ranges from 2 colours in mode 2 to 16 colours in mode 0. In addition to loading the colours an extra colour data byte must be sent to this channel to define the border colour. On power-up and other system resets the contents of the palette are undefined, but the border colour is set to BLACK, to avoid unsightly effects on power-up.

The 32 colour codes are decoded to drive the RGB signals, producing 27 different colours. The hardware colours are listed in Appendix V.

G. m8255 Parallel Peripheral Interface.

The PPI as well as the 8 port pins on the PSG are used to interface to the keyboard and to control and sense miscellaneous signals on the processor board. Port A must be programmed either to input or to output in mode 0 since this port is used for reading and writing to the PSG. Port B must be programmed to input in mode 0. Port C must be programmed to output in mode 0 on both halves.

Circuitry is provided around the PPI to reset it during system reset. For details of the operation of the µPD8255 see the NEC product specification.

CHANNEL A (Input or Output)

Bit 7:	Data/Address DA7 connected to AY-3-8912.
Bit 6:	Data/Address DA6 connected to AY-3-8912.
Bit 5:	Data/Address DA5 connected to AY-3-8912.
Bit 4:	Data/Address DA4 connected to AY-3-8912.
Bit 3:	Data/Address DA3 connected to AY-3-8912.
Bit 2:	Data/Address DA2 connected to AY-3-8912.
Bit 1:	Data/Address DA1 connected to AY-3-8912.
Bit 0:	Data/Address DA0 connected to AY-3-8912.

CHANNEL B (Input Only)

Bit 7:	Datacorder cassette read data.
Bit 6:	Centronics busy signal.
Bit 5:	Not expansion port active signal.
Bit 4:	Not option link LK4.
Bit 3:	Not option link LK3.
Bit 2:	Not option link LK2.
Bit 1:	Not option link LK1.
Bit 0:	Frame flyback pulse.

The option links, LK1..LK4 are factory set. LK4 is fitted for 60 Hz T.V. standards and omitted for 50 Hz standards.

CHANNEL C (Output Only)

Bit 7:	AY-3-8912 BDIR signal.
Bit 6:	AY-3-8912 BC1 signal.
Bit 5:	Datacorder cassette write data
Bit 4:	Datacorder cassette motor on.
Bit 3:	Keyboard row select KR3.
Bit 2:	Keyboard row select KR2.
Bit 1:	Keyboard row select KR1.
Bit 0:	Keyboard row select KR0.

H. Centronics Port Latch.

This latch is loaded with data by output commands to the correct I/O channel. It cannot be read. Note that the timing requirements on Centronics interfaces generally specify that the data must be present on the seven data lines at least 1 microsecond before the strobe is made active and must remain valid for at least 1 microsecond after the strobe returns inactive. The duration of the strobe must be between 1 and 500 microseconds. The busy signal can be inspected as soon as the strobe is inactive in order to determine when more data can be sent.

Bit 7:	Centronics strobe signal (1 = active)
Bit 6:	Data 7 to Centronics port.
Bit 5:	Data 6 to Centronics port.
Bit 4:	Data 5 to Centronics port.
Bit 3:	Data 4 to Centronics port.
Bit 2:	Data 3 to Centronics port.
Bit 1:	Data 2 to Centronics port.
Bit 0:	Data 1 to Centronics port.

On power-up and other system resets the outputs of this latch are all cleared.

I. Keyboard and joysticks.

The keyboard and Joystick switches are sensed by selecting one of ten rows using the four control bits on channel C of the PPI and reading the data from the I'SG parallel port using port A of the PPI.

The keyboard and joystick switches are arranged in a 10 by 8 matrix. One of ten rows is selected using the code on KR0..KR3 and the eight bits of data are then read in parallel on a parallel port as described above. A switch is active (closed) if the corresponding data bit is a logic 0.

The key number associated with each key (see Appendix 1) is constructed as follows:

Bit:	7	6	5	4	3	2	1	0
	0	Row number				Bit number		

Thus the key that is associated with bit 5 in row 4 has key number 37 (4*8+5).