TMS 3556
VIDEO DISPLAY PROCESSOR

Features

- Generation and control of displayed colour television image.
- 320 × 250 resolution on TV screen.
- 8 colours.
- Mask programmable display characteristics.
- External synchronisation capability.
- Asynchronous DMA technique used for memory access.
- High speed memory input channel for teletext data.
- Automatic refresh for dynamic RAM.
- Text, graphic and mixed mode capability.
- Multipage capability.
- 4 × 128 character generator capability.
- 40 pin DIL plastic or ceramic package.
- 5V & 3V power supplies.

Description

The TMS 3556 Video Display Processor (VDP) is an N channel MOS LSI device used in video systems to generate a colour television image. Transparent asynchronous direct memory access technique for memory access allows the VDP to be easily used in Teletext or Videotex applications.

The VDP interfaces with the CPU via an 8 bit bidirectional data bus. Automatic RAS/CAS generation and refresh of dynamic RAM allow large memories (up to 64K bytes) at low cost.

The VDP has three video display modes: Text, graphic and mixed mode.

- Text mode provides 25 rows of 40 characters, each character is displayed in two colours and in an 8 by 10 matrix.
- Graphic mode provides a 320 x 250 pixel display. The colour of each pixel can be independently defined.
- Mixed mode provides a combination of the two above modes.

TMS 3556
40 PIN 600 MIL PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)

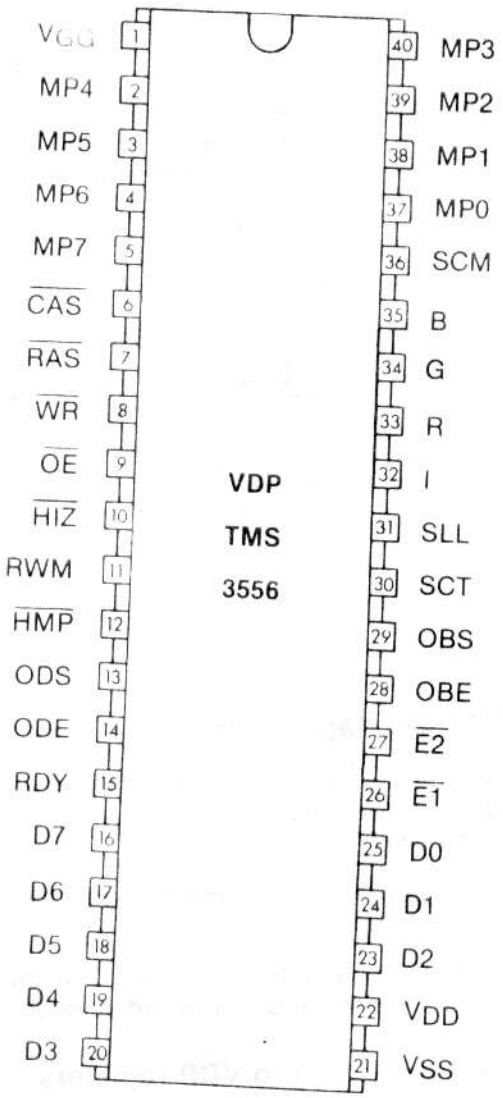


FIGURE 1

Absolute maximum ratings

Supply voltage Vgg . . . . . – 0.3 to 10V
Supply voltage Vdd . . . . . – 0.3 to 10V
High level input voltage Vih . . . . . .
Operating free air temperature range . 0 to 60°C
Storage temperature . . . . . – 55 to + 140°C

All voltage[s] [with] respect to Vss.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

TEXAS INSTRUMENTS

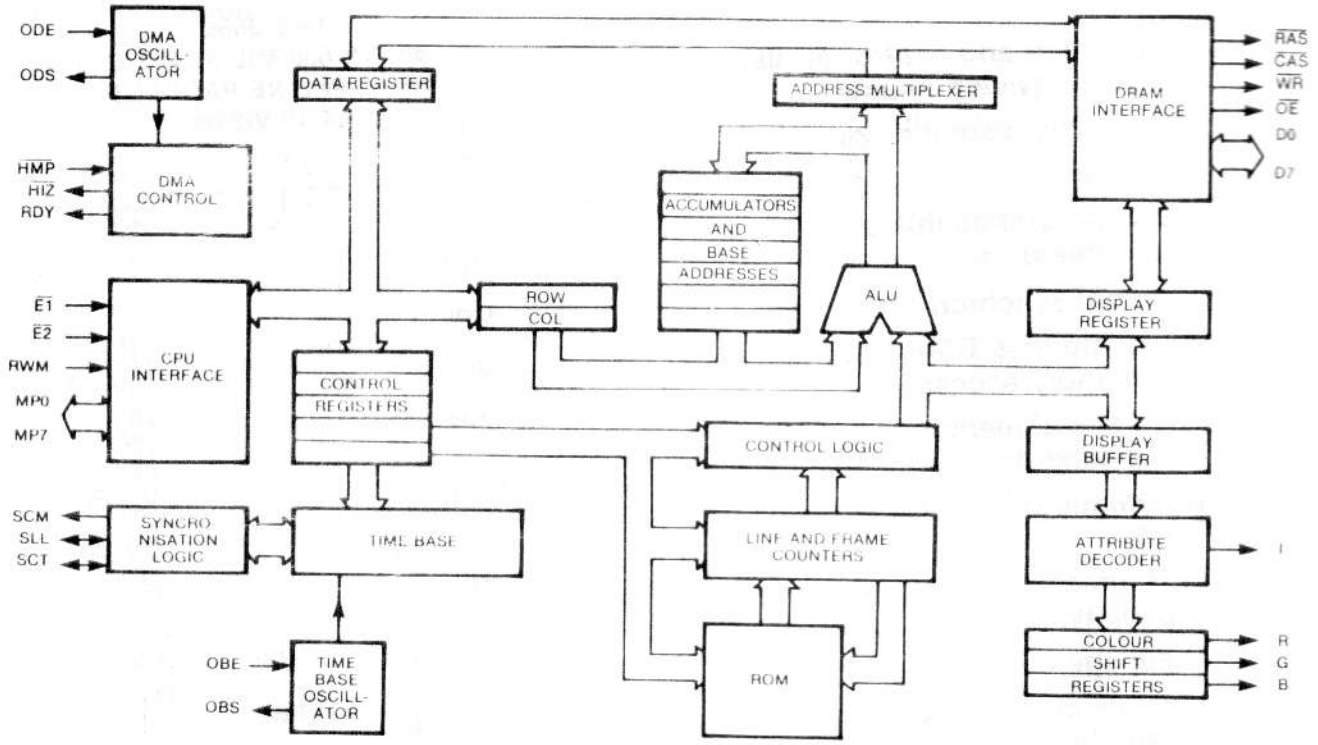


FIGURE 2: BLOCK DIAGRAM OF TMS 3556 VDP

1.1 - CPU interface control signals

The type and direction of data transfers are controlled by the $\overline{E1}$, $\overline{E2}$ & **RWM** Inputs. When $\overline{E1}$ and $\overline{E2}$ are high, the CPU interface is in the inactive state. All data transfers are performed on an 8 bit bidirectional bus **MP0-MP7**.

The $\overline{E1}$ and $\overline{E2}$ signals must return to the inactive state before a new access is requested (see table below).

The **RDY** signal indicates to the CPU that valid data is available on the **MP** bus in the case of a read access, or that the CPU channel is occupied following a write access.

1.2 - CPU write/read to VDP registers

The VDP has 15 write-only registers and one read only status register. The write registers control VDP operation (mode, border colour, TV standard selection, insertion, etc...) and determine the base addresses used by the VDP to control its video RAM; the status register contains information on frame synchronisation, buffer status (overflow or empty), memory access and horizontal and vertical display intervals.

1.3 - CPU write/read to the video RAM

The CPU transfers data to the VRAM through the VDP using a 16 bit autoincrementing address pointer. Four byte transfers are required to initialise the address pointer (cycles to write to VDP registers **COL** & **ROW**) and thereafter one byte transfer is needed for each transfer of data to the addressed VRAM bytes (write to VRAM cycles).

The same operation is performed to read the VRAM but $\overline{E1}$, $\overline{E2}$ & **RWM** inputs are asserted in the read mode.

1.4 - VDP/VRAM interface

The VDP can access up to 64K bytes of VRAM. It provides all necessary signals to interface with dynamic RAM (**$\overline{RAS}$, $\overline{CAS}$, $\overline{WR}$, $\overline{OE}$** and multiplexed address and data on the bidirectional bus **D0-D7**). The VDP automatically refreshes the VRAM. The VDP is compatible with all currently available dynamic memories including: the TMS4164 (64K × 1), TMS4416 (16K × 4), TMS4116 (16K × 1), TMS4408 (8K × 4).

TABLE 1 - CPU/VDP DATA TRANSFERS

OPERATION	$\overline{E1}$	$\overline{E2}$	R/W
Interface disabled	1	1	X
Read VRAM	0	0	1
Write VRAM	1	0	0
Read VDP register	0	1	1
Write VDP register	0	1	0

(X means don't care)

2.1 - Description of internal registers

Registers 0 to 7 define the state of the VDP, registers 8 to 15 defined the value of base addresses.

VDP REGISTERS

REGISTER	ADDRESS (HEX)	CONTENTS	BIT ASSIGNMENT							
			MSB M0	M1	M2	M3	M4	M5	M6	LSB M7
Pointer	0	Access address	RT8	RT4	RT2	RT1	AC8	AC4	AC2	AC1
COL	1	Column address	A8	A9	A10	A11	A12	A13	A14	A15
ROW	2	Row address	A0	A1	A2	A3	A4	A5	A6	A7
STAT	3	Status register	ST1	ST2	ST3	ST4	ST5	ST6	ST7	ST8
CM1	4	Time base	BT1	BT2	BT3	BT4	BT5	X	X	X
CM2	5	Decoder	DC1	DC2	DC3	DC4	DC5	DC6	DC7	DC8
CM3	6	Control unit	CT1	CT2	CT3	CT4	CT5	CT6	X	X
CM4	7	Border colour	BM	VM	RM	X	MR	LR	IR	X
		BASE ADDRESSES								
BAMT	8	Start of buffer								
BAMP	9	CPU address register								
BAPA	A	Page display memory								
BAGC0	B	Character generator 0								
BAGC1	C	Character generator 1								
BAGC2	D	Character generator 2								
BAGC3	E	Character generator 3								
BAMTF	F	End of buffer								

2.2.1 - Register 0

Register 0 is the register pointer. **AC8-AC1** contain the address of the register to be accessed. The value of **RT8-RT1** is copied into **AC8-AC1** following the access and may either point to the pointer (value = 0) or to another register.

2.2.2 - Register 1

Register 1 is a temporary store containing the column address for a VRAM or base address access (LS byte).

2.2.3 - Register 2

Register 2 is a temporary store containing the row address for a VRAM or base address access (MS byte).

2.2.4 - Register 3

Register 3 contains VDP status information.

ST1	ST2	ST3	ST4	ST5	ST6	ST7	ST8
Not used	Frame sync.	Vertical display interval	Not used	Ready	Horizontal display interval	Buffer overflow	Buffer empty

2.2.5 - Register 4

Register 4 controls the time base.

BT1	BT2	BT3	BT4	BT5
Frame interlacing	TV standard	Not used	Combined with DC1 to select SLL&SCT mode	Sub-titling mode

2.2.6 - Register 5

Register 5 controls the decoder.

DC1	DC2	DC3	DC4	DC5	DC6	DC7	DC8
Internal sync.	Display of row 0	Masking enable	Insertion enable	Mosaic/ alphanum Chr.Gen3	Grid display	Underlining enable	Super-position enable

2.2.7 - Register 6

Register 6 defines display modes, type of DRAM and memory timing.

CT1	CT2	CT3	CT4	CT5	CT6
Graphic mode	Text mode	not used	CPU access disabled during display interval	Memory timing	DRAM type

2.2.8 - Register 7

The register 6 contains full page attributes.

BM	GM	RM	MR	LR	IR
Blue	Green	Red	Full page masking	Full page underlining	Full page insertion
border colour					

2.2.9 - Register 8 to 15

Register 8 to 15 define the organisation of the VDP RAM.

BAMT and **BAMTF** define the location of the buffer in the VRAM.
BAGCO to **BAGC3** define the location of the character generators.
BAPA defines the location of the page display memory.
BAMP is used to transfer addresses into the second CPU address pointer.

3.1 - Video display modes

The VDP displays an image on the TV screen that is a combination of information provided by its VRAM and internal registers.

3.2.1 - Text mode

Text mode is designed for terminals producing alpha-mosaic type displays.

The screen is composed of typically 25 rows of 40 characters. The characters may be alpha-numeric or block graphic. Characters from up to four independent character generators each containing 128 different characters are allowed on one display screen.

Characters may be flashed, inversed, underlined, masked, displayed in double width, double height or double size. The may also be superimposed onto an automatically synchronised external video signal.

Additionally in this mode the margin colour is stored in register CM4 together with full page masking, underlining and incrustation attributes.

3.2.2 - Graphic mode

Bit-mapped mode is designed for terminals producing alpha-geometric type displays.

Each dot on the display screen, typically 320 points by 250 lines, is individually programmable in one of eight colours.

Register **CM4** has no effect in this mode, the colour of the margin being defined in the page memory at the end of each line of display data.

3.2.3 - Mixed mode

The above two modes of operation may be mixed on a line by line basis on the same screen. Since text mode required less memory space than bit-mapped mode, this mode enables economy of VRAM in applications where full bit-map is not required over the whole screen.

4.1 - DMA functionnal description

The asynchronous DMA system allows access to a common external memory through three separate channels. The 3 types of VRAM access are as follows: display, data processing by the CPU and data loading by the data provider. The accesses requested are stored in the DMA controller then executed according to the following priority ranking — 1) data provider, 2) processing unit, 3) display.

HMP and $\overline{\text{HIZ}}$ control signals are used for data transfer from the data provider to the buffer in VRAM through the data bus **(DO-D7)**. **HMP** (input) is a byte clock and $\overline{\text{HIZ}}$ (output) a transfer enable signal.

4.2 · Description of autoincrementing pointers

The VDP contains several auto-incrementing address pointers for memory accesses. These pointers enable the various elements of the system: CPU, data provider, display controller etc. to access the memory on an incremental basis without explicitly redefining the access address. Two pointers are associated with CPU accesses: **ACMP** and **ACMPxy.** Both these pointers may be initialised by the CPU and thereafter the latter may simply make read or write accesses to the memory continuously without redefining its access address.

For more details on auto-incrementing pointers, reference should be made to the TMS3556 family users manual.

5 · Electrical specification

5.1 · Absolute maximum ratings

Supply voltage Vgg ..... – 0.3 to 10 V
Supply voltage Vdd ..... – 0.3 to 10 V
All input voltages ..... – 0.3 to 10 V
Continuous power dissipation ..... 1 W
Operating free air temperature range ..... 0 to 60 C
Storage temperature range ..... – 55 to + 140 C
Maximum short circuit output current .....

All voltages are with respect to Vss

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this data sheet is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 · Recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage Vgg		4.75	5	5.25	V
Supply voltage Vdd		2.85	3	3.15	V
Supply voltage Vss			0		V
High-level input voltage, (all inputs except OBE and ODE)	Vih	2.2		5.25	V
High-level input voltage (OBE and ODE inputs)		2.7		5.25	V
Low level input voltage, (all inputs exept OBE and ODE)	Vil	0		0.8	V
Low level input voltage (OBE and ODE inputs)		0		0.6	V
Low level output current (SCM, SLL & SCT outputs)					mA
Operating free air temp.,	Ta	0		60	C

5.3 - Electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voh	High-level Output voltage	RAS, CAS, OE WR, D(0 – 7)	Ioh = 1.5mA	2.4			V
		MP(0 – 7) HIZ	Ioh = 500uA	2.4			V
		READY	Ioh = 250uA	2.4			V
		R,G,B,I	Ioh = 500uA	2.4			V
Vol	Low level Output Voltage	RAS, CAS, OE WR, D(0 – 7)	Iol = 3.5mA			0.6	V
		MP(0 – 7) HIZ	IoL = 1.0mA			0.6	V
		READY	Iol = 500uA			0.6	V
		R,G,B,I	Iol = 2.0mA			0.6	V
		SCM,SCT,SLL	Iol = 2.0mA			0.6	V
Iih	High level Input current	D(0 – 7)	Vi = 5.25V			100	uA
		MP(0 – 7)				200	uA
		All others				10	uA
Iil	Low level Input current	D(0 – 7)	Vi = 0V			– 100	uA
		MP(0 – 7)				– 200	uA
		All others				– 10	uA
Iozh	Off-state output current, high level voltage applied	D(0 – 7)	Vo = 5.25V			100	uA
		MP(0 – 7)	Vo = 5.25V			200	uA
Iozl	Off-state output current, low level voltage applied	D(0 – 7)	Vo = 0.4V			– 100	uA
		MP(0 – 7)	Vo = 0.4V			– 200	uA
Igg	Supply current from Vgg		Vgg = MAX		105	140	mA
Idd	Supply current from Vdd		Vdd = MAX		70	100	mA
Ci	Input capacitance	MP(0 – 7) D(0 – 7)	f = 1 Mhz			15	pF
		All others	f = 1 MHz			10	pF
Co	Output capacitance	MP(0 – 7) D(0 – 7)	f = 1 MHz			15	pF
		All others	f = 1 MHz			10	pF

All typical values are at Vgg = 5V, Vdd = 3 V, Ta = 25°C.

Note 1: All voltages are with respect to Vss unless otherwise noted.

5.4 - Timing requirements over full ranges of recommended operating conditions.

PARAMETER		MIN	NOM	MAX	UNIT
tc (ODE)	DMA oscillator cycle time	54.5			ns
tc (OBE)	time base oscillator cycle time	110			ns
tc (E)	E1, E2 cycle time	See users manual			
tc (HMP)	HMP cycle time	See users manual			
td (RDHEL)	delay time RDY high to E1, E2 low	0			ns
tsu (ERWL)	E1, E2 set up time before RWM low	10			ns
th (RWHE)	E1, E2 hold time after RWM high	10			ns
twh (E)	E1, E2 pulse width, E1 and E2 high	110			ns
twl (RWM)	pulse width, RWM low	110			ns
tsu (MPRWL)	data set up time before RWM low	5			ns
th (RWLMP)	data hold time after RWM low	40			ns
tsu (ELODL)	set up time, E2 low to ODE low~				ns
tsu (RWHODL)	set up time, RWM high to ODE low~				ns
tsu (DCH)	data set up time before CAS high				ns
th (CHD)	data hold time after CAS high	0			ns
tdis (CHD)	data disable time after CAS high			35	ns
twl (HMP)	pulse width HMP low	220			ns

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, Vil max and Vih min must be met at the 10% and 90% points.

~ This is a system timing parameter only and need not be respected in all cases; see users manual.

5.5 - Switching characteristics over full ranges of recommended operating conditions (Independent of DMA oscillator frequency)

PARAMETER		MIN	NOM	MAX	UNIT
tac (ST)	status register access from E1 low			140	ns
ten (ELMP)	MP bus enable time after E1, E2 low	40			ns
tsu (MPRDH)	data set up time before RDY high	5			ns
th (EHMP)	data hold time after E1, E2 high	0		50	ns
td (ELRDL)	delay time, E2 low to RDY low	45		90	ns
td (RWHRDL)	delay time, RWM high to RDY low	45		90	ns
tdis (CLD)	disable time, CAS low to Dn high z			30	ns
th (CLCA)	column address hold time after CAS low	15			ns
ten (HZHD)	enable time, HIZ high to Dn driven	20			ns
td (CHHZH)	delay time, CAS high to HIZ high			15	ns
td (DMP)	delay time, Dn valid to MPn valid		60		ns
td (ODLRL)	delay time ODE low to RAS low	20			ns
td (OBHIH)	delay time OBE high to I high	0			ns
td (OBLIL)	delay time OBE low to I low	0			ns
td (OBLRGB)	delay time OBE low to R, G, B valid				ns
th (OBLRGB)	R, G, B hold time after OBE low				ns
td (OBLSL)	delay time OBE low to SLL low	0		90	ns

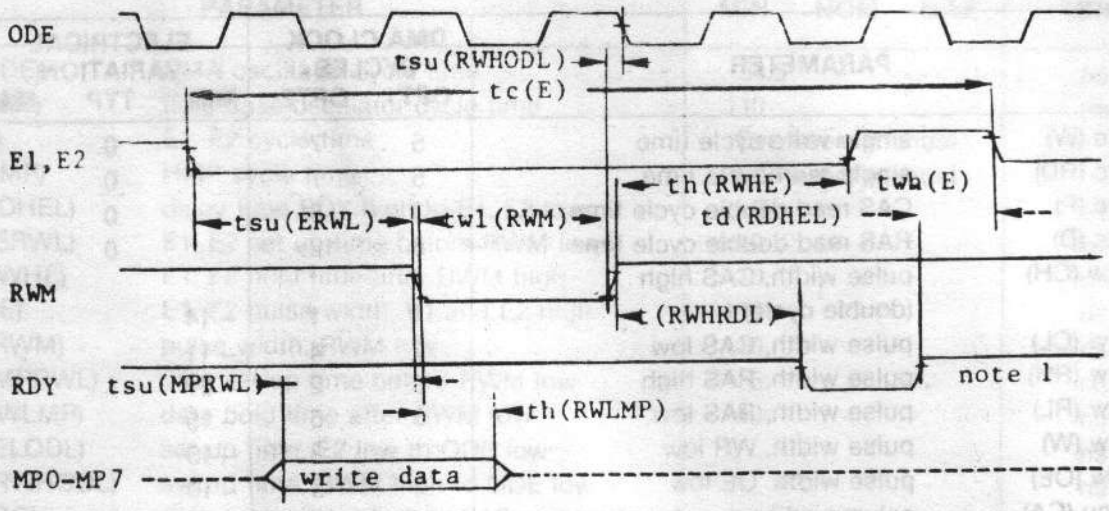
~ See user's manual TMS 3556.

5.6 - Switching characteristics over full ranges of recommended operating conditions (Dependent of DMA oscillator frequency)

PARAMETER		DMA CLOCK CYCLES OPT1	DMA CLOCK CYCLES OPT2	ELECTRICAL VARIATION MIN	ELECTRICAL VARIATION TYP	ELECTRICAL VARIATION MAX	UNIT
tc (W)	single write cycle time	5	7		0		ns
tc (RD)	single read cycle time	5	7		0		ns
tc (P)	CAS read double cycle time	3	5		0		ns
tc (D)	RAS read double cycle time	8	12		0		ns
tw (CH)	pulse width, CAS high (double cycle)	1	1	– 14			ns
tw (CL)	pulse width, CAS low	2	4	– 11			ns
tw (RH)	pulse width, RAS high	2	2	– 21			ns
tw (RL)	pulse width, RAS low	3	5	– 15			ns
tw (W)	pulse width, WR low	1	3	– 10			ns
tw (OE)	pulse width, OE low	1	3	– 10			ns
tsu (CA)	column address set up time	0.5	0.5	– 27			ns
tsu (RA)	row address set up time	1	1	– 45			ns
tsu (D)	data set up time before WR low	0.5	0.5	– 20			ns
tsu (WRH)	WR set up time before RAS high	1	3	– 15			ns
tsu (WCH)	WR set up time before CAS high	1	3	– 15			ns
tsu (ORH)	OE set up time before RAS high	1	3	– 15			ns
tsu (OCH)	OE set up time before CAS high	1	3	– 15			ns
th (RA)	row address hold time after RAS low	0.5	0.5	0			ns
th (WLD)	data hold time after WR low	1	3	30			ns
td (RLCL)	delay time, RAS low to CAS low	1	1	– 10			ns
td (CLWL)	delay time, CAS low to WR low	1	1	– 15			ns
td (HZLCL)	delay time, HIZ low to CAS low	2	2	15			ns
tac (E)	read access time from E2 low ~						
td (ELRL)	delay time, E2 low to RAS low ~						
td (RWHRL)	delay time, RWM high to RAS low ~						
td (HPLHZL)	delay time, HMP low to HIZ low ~						

~ See TMS 3556 users manual.

FIGURE 5.1: CPU - VDP WRITE CYCLE TIMING



Note 1: Ready stays high for accesses to registers 0 to 7

FIGURE 5.2: CPU - VDP MEMORY READ CYCLE TIMING

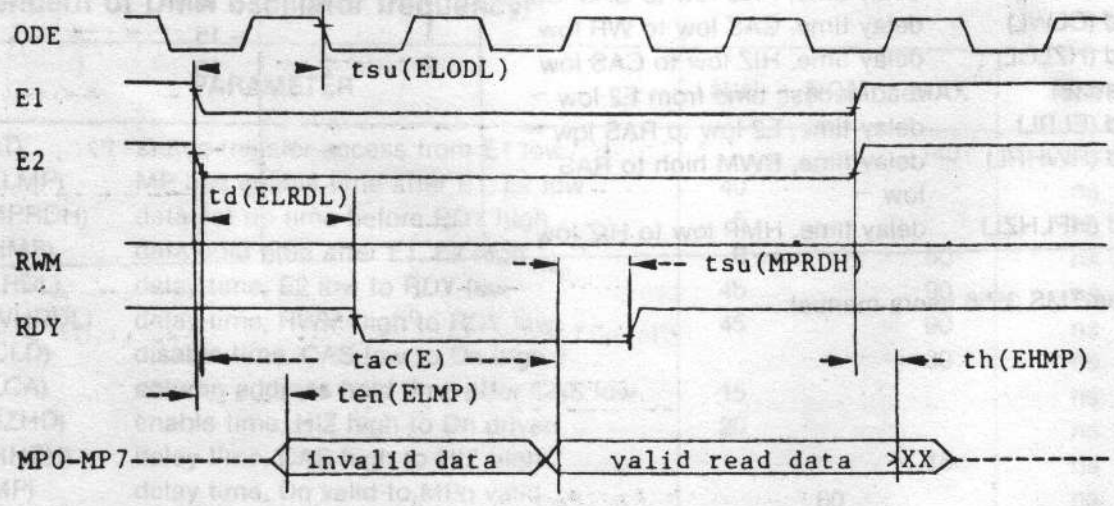


FIGURE 5.3: CPU - VDP STATUS READ CYCLE TIMING

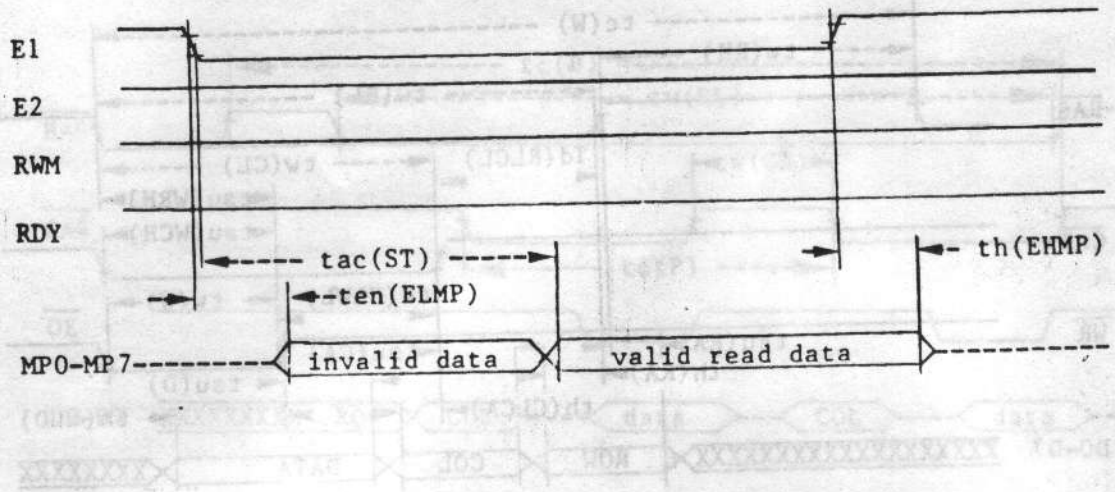
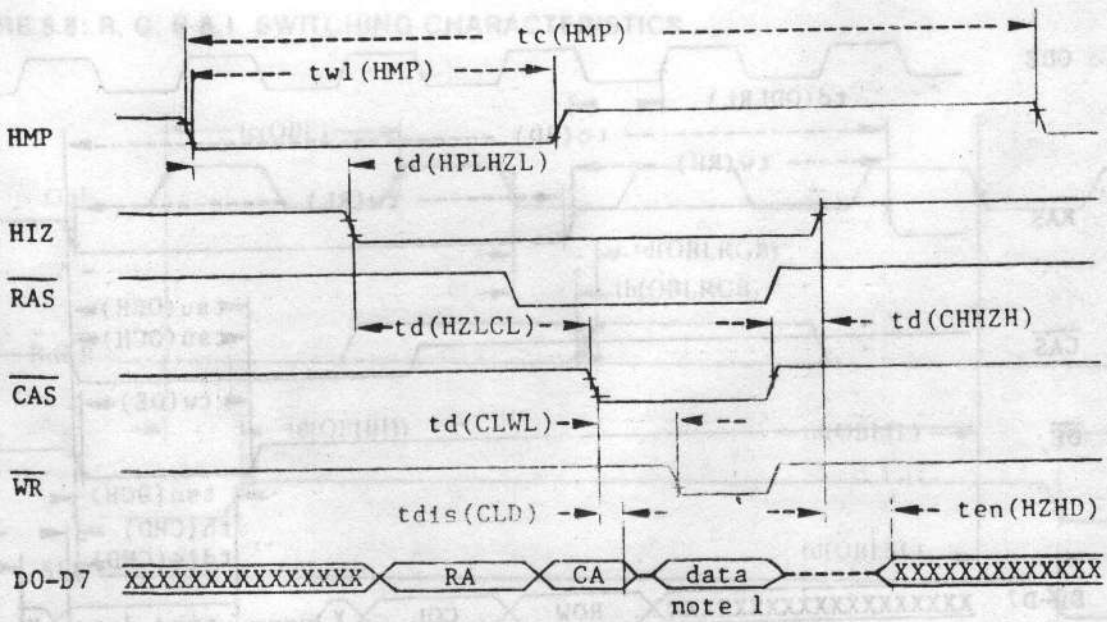


FIGURE 5.4: DATA PROVIDER WRITE CYCLE TIMING



Note 1: VDP MP bus is high impedance, data is output by the data provider. Data set-up and hold times with respect to WR are determined by memory timing requirements.

FIGURE 5.5: VDP - DRAM WRITE CYCLE TIMING

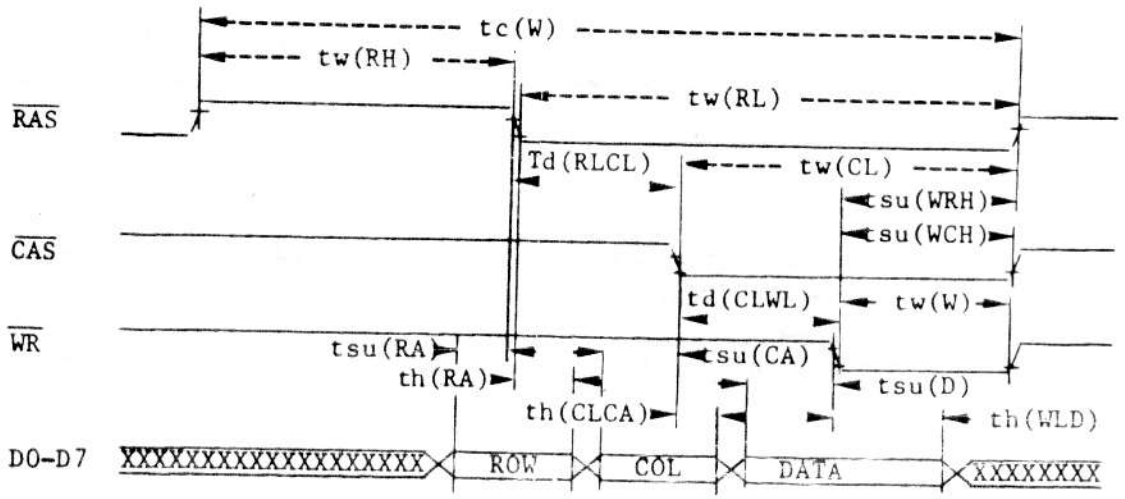
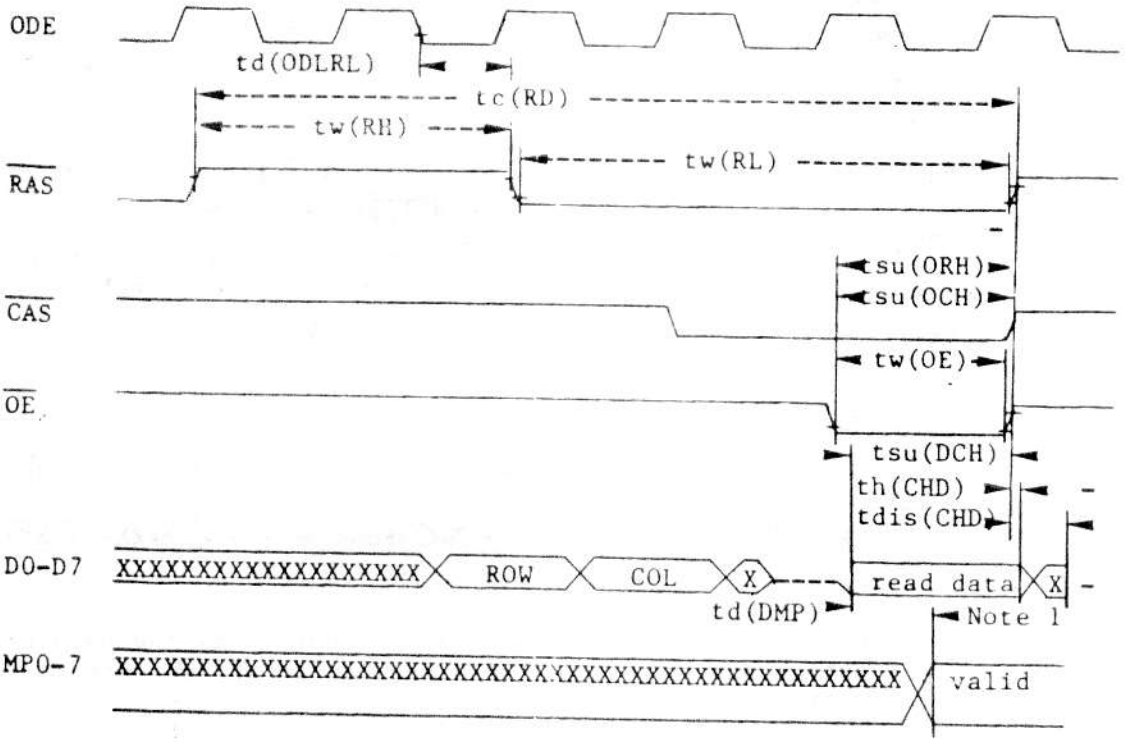


FIGURE 5.6: VDP - DRAM READ CYCLE TIMING



Note 1: td(DMP) applies to CPU memory read cycles only

FIGURE 5.7: VDP - DRAM DOUBLE READ CYCLE TIMING

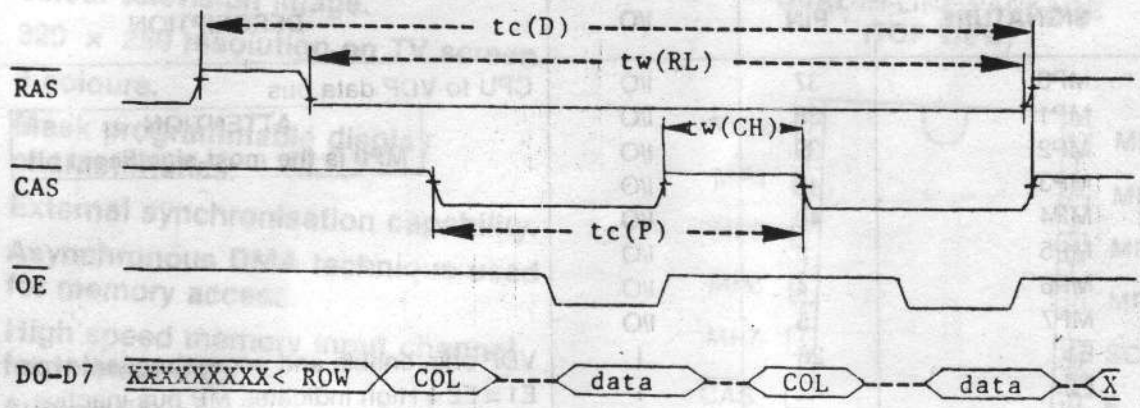
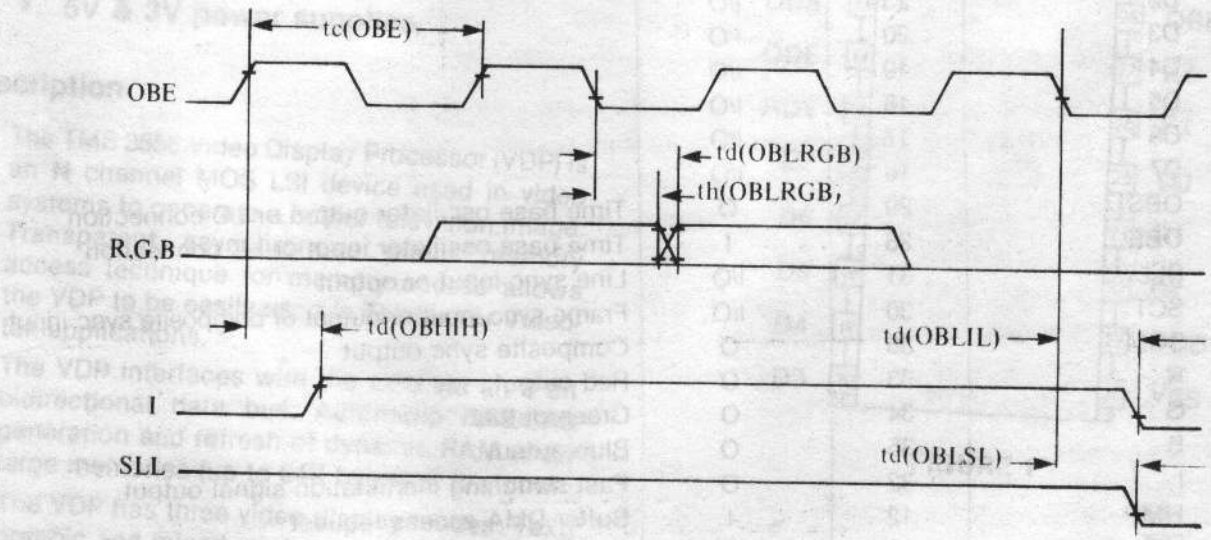


FIGURE 5.8: R, G, B & I SWITCHING CHARACTERISTICS



6 - Pin description

SIGNATURE	PIN	I/O	DESCRIPTION
MP0	37	I/O	CPU to VDP data bus
MP1	38	I/O	**ATTENTION**
MP2	39	I/O	**MP0 is the most significant bit**
MP3	40	I/O	
MP4	42	I/O	
MP5	3	I/O	
MP6	4	I/O	
MP7	5	I/O	
$\overline{E1}$	26	I	VDP chip enable and access request type
$\overline{E2}$	27	I	E1 = E2 = High indicates MP bus inactive
RWM	11	I	CPU data write strobe
RDY	15	O	CPU access ready signal
ODS	13	O	DMA clock oscillator output or LC connection
ODE	14	I	DMA clock oscillator input or LC connection
$\overline{RAS}$	7	O	VRAM row address strobe
$\overline{CAS}$	6	O	VRAM column address strobe
$\overline{WR}$	8	O	VRAM data write strobe
$\overline{OE}$	9	O	VRAM output enable
D0	25	I/O	VRAM multiplexed address/data/
D1	24	I/O	DO is the most significant bit
D2	23	I/O	
D3	20	I/O	
D4	19	I/O	
D5	18	I/O	
D6	17	I/O	
D7	16	I/O	
OBS	29	O	Time base oscillator output or LC connection
OBE	28	I	Time base oscillator input or LC connection
SLL	31	I/O	Line sync input or output
SCT	30	I/O	Frame sync input or output or composite sync input
SCM	36	O	Composite sync output
R	33	O	Red output
G	34	O	Green output
B	35	O	Blue output
I	32	O	Fast switching incrustation signal output
HMP	12	I	Buffer DMA access request
$\overline{HIZ}$	10	O	Buffer DMA access grant
VGG	1	I	5V supply voltage
VDD	22	I	3V supply voltage
VSS	21	I	Ground reference