6502 Dead Cycles[1] Opcode/Addressing Mode	Cycle[2,3]	Internal Operation[4]	External Operation 6502[15]	External Operation 65C02[15]
1. zpg,X/Y	3	BAL + X	PFA[6]	PBA[7]
2. abs,X/Y – read w/ pg. crossing	4*	BAH + 1	PFA	PBA
3. abs,X/Y – write w/o pg. crossing[8]	4	BAH + 0	FFA[5,8]	FFA[5,8]
4. abs,X/Y – write w/ pg. crossing	4	BAH + 1	PFA	PBA
5. (zpg),Y – read w/ pg. crossing	5*	BAH + 1	PFA	PBA
6. (zpg),Y – write w/o pg.crossing	5	BAH + 0	FFA	PBA
7. (zpg),Y – write w/ pg.crossing	5	BAH + 1	PFA	PBA
8. (zpg,X)	3	BAL + X	PFA	PBA
9. RMW zpg,X – "Read, Modify, Write" Opcodes[11]	3	BAL + X	PFA	PBA
10. RMW abs,X – 6502 w/o pg. crossing	4	BAH + 0	FFA	
11. RMW abs,X – 6502 w/ pg. crossing	4	BAH + 1	PFA	
12. RMW abs,X – 65C02 INC/DEC w/o pg. crossing	4	BAH + 0		FFA
13. RMW abs,X – 65C02 INC/DEC w/ pg. crossing	4	BAH + 1		PBA
14. RMW abs,X – 65C02 ASL LSR ROL ROR w/ pg. crossing[12]	4*	BAH + 1		PBA
15. RMW zpg	4	Modify	FFA (W)[9]	FFA
16. RMW abs	5	Modify	FFA (W)	FFA
17. RMW zpg,X	5	Modify	FFA (W)	FFA
18. RMW abs,X	6[12]	Modify	FFA (W)	FFA
19. All 1 Byte Opcodes	2	–	PC[10]	PC[10]
20. JMP (abs)/(abs,X) – 65C02	4	–		PBA
21. JSR	3	–	SP	SP
22. RTS, RTI, PLP, PLA, PLY, PLX	3	SP + 1	SP	SP
23. RTS	6	PC + 1	PC[10]	PC[10]
24. Branch (taken)[14]	3	PCL + BOF[13]	PC[10]	PC[10]
25. Branch (taken) – w/ pg. crossing[14]	4*	PCH +/- 1	PC[10]	PC[10]
26. Extra BCD Cycle – 65C02	*	BCD		PBA

[1] A Dead Cycle is one in which the CPU is busy with an internal operation and does not make specific use of the external buses.

[2] Cycle numbers are with reference to Fetch_Opcode as cycle 1.

[3] "*" denotes the cycle is added on a page crossing.

[4] BAL and BAH refer to "Base Address Low" and "Base Address High" respectively.

[5] FFA refers to a Fully Formed Address, which is the final target address of a given addressing mode.

[6] PFA refers to a Partially-Formed Address, one which has yet to be adjusted, as follows:
- zpg,X/Y — ("00", BAL) Base address before the index register is added to the low-byte (BAL doesn't yet reflect the index offset)
- abs,X/Y — (BAH, BAL+X/Y) Base address before the low-byte carry is added to the high-byte (BAH doesn't yet reflect the page crossing)
- (zpg),Y — (BAH, BAL+Y) Base address before the low-byte carry is added to the high-byte (BAH doesn't yet reflect the page crossing)
- (zpg,X) — ("00", BAL) Base address before the index register is added to the low-byte (BAL doesn't yet reflect the index offset)

[7] PBA refers to the Previous Bus Address (i.e., the value on the address bus from the previous cycle). This is the “fix” introduced by the 65C02. Re-reading the PBA is assumed to be a safe action, preferable to generating a "stray" read with an "invalid address", aka a Partially Formed Address (PFA), as the NMOS 6502 does. A PBA is also used on the 65C02 as a "safe" address for the dead cycle in JMP (abs) and the extra cycle in BCD operations.

[8] abs,X/Y write operations without a page-crossing actually read from the Fully Formed Address before writing to it. The read can be troublesome when accessing I/O devices where reads are destructive. For 65C02 there's a software workaround, which is to ensure that the write to abs,X/Y triggers a page-crossing, which means the address during the dead cycle will be a PBA, not the Fully Formed Address. The only software workaround that works on both NMOS and CMOS 6502 is to avoid abs,X/Y address mode when writing to the read-sensitive device.

[9] External Operations are Reads unless otherwise noted by "(W)".

[10] PC refers to the address at PC, as follows:
- 1-Byte Opcodes Cycle 2 — Address of next opcode
- RTS Cycle 6 — Return address - 1 (as retrieved from the stack)
- Branch (taken) Cycle 3 — Address of next opcode after Branch
- Branch (taken) w/ pg. crossing Cycle 4 — High-byte unchanged from prior cycle/Low-byte of target address (PCL + BOF[13])

[11] "Read, Write, Modify" Opcodes refers to INC, DEC, ASL, LSR, ROL and ROR.

[12] On the 65C02, the "Modify" operation occurs in cycle 5 for ASL, LSR, ROL and ROR if a page is not crossed.

[13] BOF refers to the Branch Offset value.

[14] Dead cycles are 5 and 6* for 65C02 BBR and BBS (rather than cycles 3 and 4* for standard branches).

[15] The behaviour shown for each CPU has been verified on the Visual 6502 (www.visual6502.org) and on a WDC 65C02 respectively. See also http://archive.6502.org/books/mcs6500_family_hardware_manual.pdf Appendix A.