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------------------------------------------
*    Principle of Operation and Control    *
*  of the Vortex Ram Extension SP 64-512   *
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```

The RAM memory of the VORTEX RAM-expansion (which we will refer to as "external-RAM") can be directly switched into the address range of the Z80 CPU within the CPC. However since the Z80 like most other 8-bit CPU has only a 16-bit address-bus, the total available RAM (128-576kb) can not be addressed at the same time, but only in portions of 64kb or less.
This principle of controlled switching selected portions of RAM into and out of the available address range of a given CPU is called mapping or bank-switching, and has to be applied whenever the CPU addressing range is smaller than the total amount of memory the system is supposed to handle.

By the way, this is nothing new with the CPC's, as they do mapping without RAM-expansion all the time. For example the BASIC ROM and the screen memory are occupying the same address area. of course the BASIC ROM and the sreen memory can't be addressed at the same time - it would cause an unnecessary bus-conflict on the data-bus - and that's something the Gate-Array takes care of. With additional control signals and using a so called 'configuration-port' (7FXX) it ensures to it that at a given time there is only out of several possible paralell RAM-areas selected. For example either screen-memory or BASIC-ROM.
It's easy to understand that the mere 16 bit address range is not sufficient for selection of a certain address within a certain bank.

The external RAM of the VORTEX expansions can be handled in 32kb blocks that can be switched in and out of the Z80 addressing range. (see picture). the control is exercised by two ports:

- Bankselect / RAMcard Enable : Port FBBD
- Blockselect/ Mapping Enable : Port 7FXX ← OUT(C),C uniquement !

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-----------------------------------------------------------------
* Definitions :                                                 *
* -------------                                                 *
* Bank :  a 64kb area of contigious memory,  which occupies     *
*         the whole addressing range (0000 to FFFF ) of the Z80 *
*         CPU. Such a bank can be switched 'on' or 'off' depen- *
*         ding on other criterion. ( 'soft-switch').            *
*                                                               *
* Block: a 32 kb area of memory. Each Bank consists of two      *
*         ' Blocks ', a lower Block (address 0000 - 7FFF )      *
*        and an upper 'Block'      (address 8000 - FFFF )       *
-----------------------------------------------------------------
```

(1) Bankselect : FBBD (port address)

The RAM - Extension has a bankselect-register that can only be written to.
This register still has nothing to do with the actual memory read/write operations, but is only the 'soft-

switch' which helps to extend the addressing range of the Z80.

However there is still more to this register, it also contains the 'switch' which enables the board.
The different bits of the bankselect register have the following effect :

Bit	Effect
0,1,2	Bankselect - chooses one of the maximum of 8 possible banks of 64kb for the following RAM-operation. These three bits help to expand the Z80 address to a virtuell range of 19 bits (or 512 kb) 0 --) Bank 0 ; 1 --) Bank 1 ; etc.
3	RAMexpansion - ROM disable; 0 = enable ROM 1 = disable ROM
4	RAM - disable~~, a '1'~~ disables all internal and external RAM. Data fetch is only possible from the ROM's. Before this bit is activated you should ensure that in the following course no RAM-read- or write operation is required. (attention : a call, nnnn, will need the RAM-stack !). This control-bit is normally not needed and is reserved for later use.
5	RAMcard - RAM disable; 0 = Disable 1 = Enable This bit can be called the 'main switch' of the board. If it is not activated, the 'mapping bit' of port 7FXX (see later) will be of no effect: The board can not be activated. This control bit has been especially designed because of certain cassette software - mainly games which have a special loader which makes use of the gate array port. If the RAM-board isn't switched off before loading these games a system crash occurs.

Normally only bit 0,1,2,5 are needed when working with the board. Bit 3 and 4 are reserved for special applications and will crash the system if not properly used.

NOTE : SEUL OUT(C),r est valable

(2) Blockselect / Mapping Enable : 7FXX (port)

The port 7FXX is used with all CPC's for controlling the gate array and serves many purposes. (colour selection, screen-mode selection, and ROM configuration). The last example indicates that the gate array also takes over certain memory mapping functions. Certain bits of this port are not used by the gate array and will be used for controlling the RAM-expansion.

Bit	Effect
6	Blockselect - selects the lower or upper block of the currently selected bank.
5	Mapping Enable - a '1' switches the block selected by bit 6 and the bank number (bit 0-2 of port FBBD) in the address range of the Z80, and disables the corresponding block of the internal RAM.

Interrupts and the VORTEX RAM EXTENSION

Definition: The Z80 CPU has a input-control signal which makes it possible to interrupt a currently running program from 'out side' in order to branch to a given memory location.

To all CPC's the interrupt is a sort of 'lifestream'. This somewhat curious statement means that all essential control functions are principally based upon the interrupt. The sole source for interrupts in the CPC (if there are no other peripherals) is the gate array. This device requests an interrupt from the Z80 300 times every second. In case the system-firmware would serve all these interrupts without further evaluation the computer would be hopelessly slowed down, busy serving inter-rupts. For this reason the system-firmware supports an event queue with priority structure. In this way the system is only insignificantly slowed down. (see the firmware book of the CPC)

The Z80 can be operated in three different interrupt modes: IM 0, IM 1 and IM 2.
These modes differ in the way the Z80 reacts to an interrupt request. With the CPC's the interrupt mode 1 (IM 1) is used. This is actualy the least flexible interuptmode, however the hardware requirements are smallest.
If the Z80 in the CPC accepts an interrupt, the running microprogram is stopped and further program execution branches to address 0038 (Hex). Here it finds a pointer to the corresponding routine which is supposed to handle the interrupt.
This pointer must never be changed without thorough consideration since otherwise the system crashes immediately. This circumstance must be carefully considered when the user himself is directly working with the expansion without making use of the software (BOS and CP/M Patch) which is delivered with the VORTEX - board. For example anytime memory blocks of the board are switched on or off the interrupt has to be disabled (DI) and to be checked to ensure that when re-enabled it will not "jump to nowhere".
In case the expansion is merely used for data-storage, meaning the program never runs in the external RAM, control of the board is comparatively simple. However when the intention is to actualy extend the program area, any programing must be carefully planned and checked to ensure that the interrupt is always going the 'right way'.

EXAMPLES

There follow some very simple examples in machine code, meant to give you an idea of how the VORTEX - expansion can be directly accesssed. These examples however, only touch the surface, inspire, and don't constitue completness.

1.) Data-storage in a lower block (0000 .... 7FFF) :

The controlling program and the stack have (!!!) to be located above 7FFF since the lower block will be mapped away when the external RAM is switched on, otherwise with the block switched off, the program too would be gone and control lost.

Task : Transfer a block of data from the buffer 'BUFF' in the lower block of bank 0 starting with address 0. (the buffer has of course to be somewhere above 7FFF). Please note that under machine code 'bank 0' refers to the first external bank since '0' is their actual physical address. (see picture sheets).

```
SELECT    EQU 0FBBDH          ; BANKSELECT PORT OF BOARD
BUFF      EQU 0F000H          ; DATABUFFER

          ORG 8000H           ; OR A HIGHER STARTADDRESS
          LD (SSTACK),SP      ; SAVE STACKPOINTER
          LD SP;SSTACK        ; AND ESTABLISH LOCAL STACK
                              ; ABOVE (8000H)
;
; CHOOSE NOW AN EXTERNAL BANK
;
          LD BC,SELECT        ; 2 BYTE PORTADDRESS FOR BANKSELECT
          LD A,00100000b      ; CHOOSE BANK 0
                              ; ENABLE RAM-BOARD (BIT 5=1)
          OUT (C),A           ; WRITE TO BANK SELECT REGISTER
                              ; OF THE BOARD
;
;Remark:  Until the next OUT to the bankselect port bank 0 is
;         selected, that means the configuration remains until
;         another bank is selected.
;
; SELECT NOW THE LOWER BLOCK AND SWITCH ON THE EXTERNAL RAM
;
          DI                  ; DISABLE INTERRUPT DURING
                              ; DATATRANSFER
          EXX                 ; SWITCH TO 2. SET OF REGISTERS
;
;-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.

          PUSH BC             ; SAVE GATE ARRAY STATUS
          RES 6,C             ; SELECT LOWER BLOCK
          SET 5,C             ; SWITCH ON EXTERNAL RAM
          OUT (C),C           ;
```

```
; EXTERNAL RAM IS NOW SELECTED --> DATA MAY NOW BE TRANSFERED
;
;
          LD HL,BUFF          ; POINTER TO BUFFER
          LD DE,0             ; DESTINATION ADDRESS IN BANK 0
          LD BC,128           ; TRANSFER 128 BYTES
          LDIR                ; MOVE BLOCK

;-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-
;
; NOW EXTERNAL RAM IS GOING TO BE AGAIN DISABLED
;
          POP BC              ; FETCH OLD GATE ARRAY STATUS
          OUT (C),C           ; AND SELECT OLD CONFIGURATION
          EXX                 ; BACK TO 1. SET OF REGISTERS
          EI                  ; INTERRUPT IS AGAIN ALLOWED
          LD SP,(SSTACK)      ; REESTABLISH STACK
          RET                 ; ALL DONE !
;
          DEFS 10             ; AREA FOR LOCAL STACK
SSTACK:   DEFS 2              ; SAVE HERE OLD STACKPOINTER
          END
```

Since the BC second-register always contains the current gate array status, (something special with the CPC s) the activation of the board is a rather simple task. On the other hand you have to be careful when working with the second registers of the Z80 (see firmwarebook).

Now if data is to be retrieved from the lower block of bank 0 (also comparatively easy), it's important to remember that as long as the firmware ROM is active, any read operation re-fers to him and any write operation to the RAM. Therefor this ROM must be switched off, before a read operation from the RAM can be successful. The part from the above program -.-.- between these lines .-.-.- is to be substituted as follows :

```
;.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-
          PUSH BC             ; SAVE GATE ARRY STATUS
          SET 2,C
          OUT (C),C           ; SWITCH OFF LOWER ROM
;
          RES 6,C             ; SELECT LOWER BLOCK
          SET 5,C             ; SWITCH ON EXTERNAL RAM
          OUT (C),C
;
;  Remark :  Switching off the ROM and switching on the RAM can't
;            normally be done with the same OUT (C),C since the
;            bits 5 and 6 don't interfere with any internal gate
;            array registers. Therefore the OUT is normally
;            ignored by the gate array. For that reason
;            first change ROM - and then RAM - configuration.
;
; NOW EXTERNAL RAM IS ACTIVE --> DATA MAY BE TRANSFERED:
;
          LD HL,0             ; POINTER TO DATA
          LD DE,BUFF          ; DESTINATION ADDRESS = BUFFER
          LD BC,128           ; TRANSFER 128 BYTES
          LDIR                ; MOVE BLOCK
;
;.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-.-
```

2.) Data storage in an upper block (8000 .... FFFF)

Data storage in an upper block of RAM is identical to the same operation in a lower block. The only difference - and that's easy to understand - is that the controlling routines and the stack must be located below 8000 (hex). When reading data from this block, it also has to be remembered that the ROM (this time the upper ROM) is switched off. (the upper ROM is controled by bit 3 of the gate array port. (see firmware book).

Important to know:

Of course it would also be possible to write to the blockselect port (gate array port 7FXX) without first switching to the second set of registers, but it has to be observed that the gate array status may change what would normally cause system crash. For that reason we used the bit manipulation commands of the Z80 in our examples, since they don't corrupt the remaining bits of the gate array status. The AND, OR, XOR etc commands may also be used for bit manipulation, however other array status bits are restored properly.
