C6845 CRT Controller

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AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core documentation
Design File Formats	EDIF Netlist, VHDL Source RTL (available at extra cost)
Constraints File	c6845.ucf
Verification	VHDL Testbench test vectors
Instantiation Templates	VHDL, Verilog
Reference designs and application notes	None
Additional Items	None
Simulation Tool Used	
ModelSim v5.5	
Support	
Support provided by CAST, Inc.	

Features

- Available under terms of the SignOnce IP License
- Supports Virtex™-E, Virtex-II, Spartan™-II, and Spartan-IIE devices
- Fully synchronous, synthesizable VHDL core, functionally equivalent to Motorola MC6845
- Capable of driving alphanumeric, semi-graphic, or bit-mapped graphics displays
- Wide range of programmable alphanumeric screen formats
- Programmable registers controlling output Vertical Sync (VS), Horizontal Sync (HS), and Display Enable (DE) signals
- Programmable horizontal line rate, sync pulse width and vertical frame rate
- Programmable registers controlling Memory Address (MA[13:0]) start address
- Programmable Start Address Register for Hardware Scrolling
- Programmable registers controlling Row Address (RA[4:0]) size, yielding a character row
- Programmable register controlling Normal Sync (Non-Interlace), Interlace Sync, or Interlace Sync and Video Mode

Applications

The core is suitable for implementing serial interfaces in a wide range of applications, including:

- Point-of-contact Kiosks
- Medical instrumentation
- Test and measurement instrumentation
- Industrial equipment
- Avionics
- Gaming and amusement machines

Table 1: Core Implementation Data

Supported Family	Example Device	Fmax (MHz)	Slices[1]	IOB[2]	GCLK[2]	BRAM	MULT	DCM	MGT	Design Tools
Virtex-E	XCV50E-8	88	293	48	2	0	N/A	0	N/A	ISE 4.2i
Virtex-II	XC2V80-5	134	242	48	2	0	0	0	N/A	ISE 4.2i
Spartan-II	XC2S30-6	71	293	48	2	0	N/A	0	N/A	ISE 4.2i
Spartan-IIE	XC2S50E-7	80	293	48	2	0	N/A	0	N/A	ISE 4.2i

Notes:
1. Assuming all core I/Os are routed off-chip
2. Optimized for speed

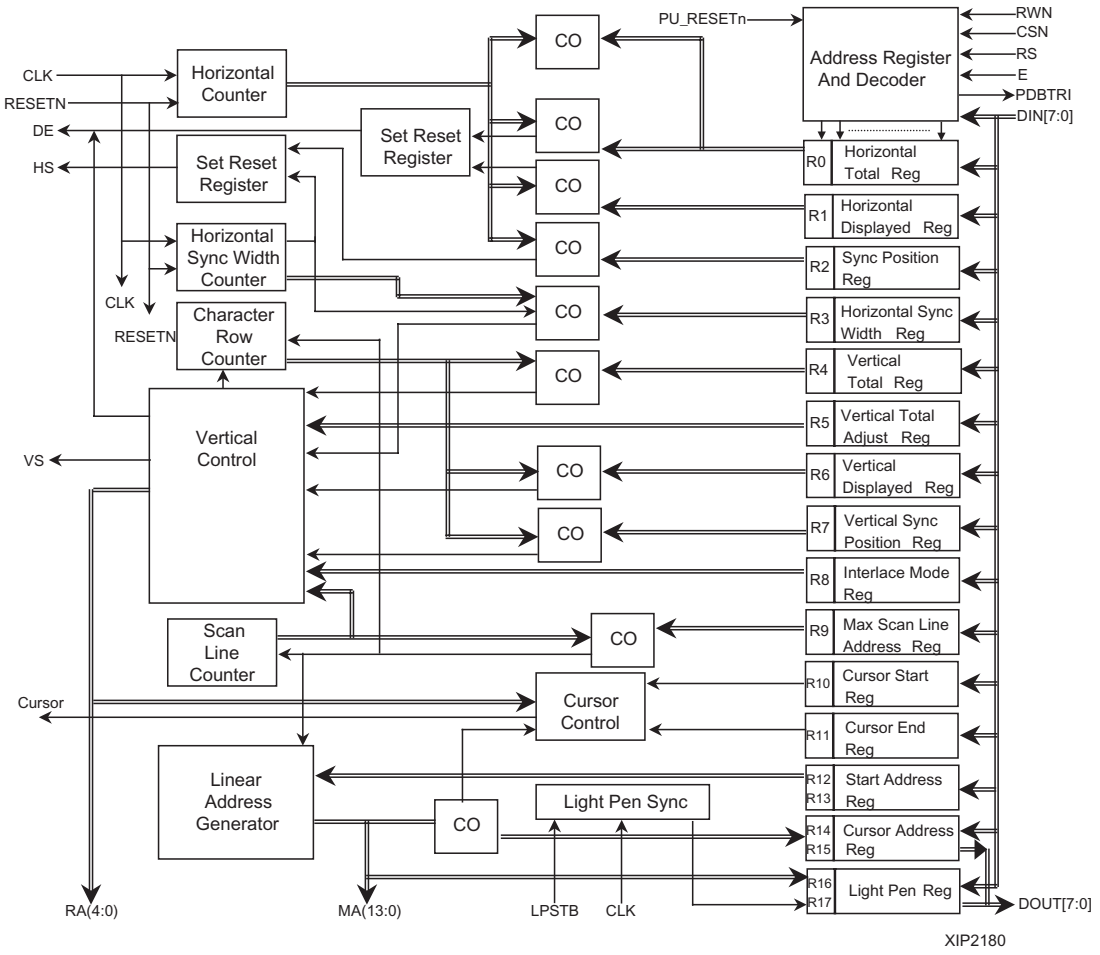

Figure 1: C6845 Core Block Diagram

General Description

The C6845 Cathode Ray Tube Controller (CRTC) interfaces a microprocessor to a raster-scan CRT display. The C6845 is a synchronous core functionally equivalent to the Motorola MC6845 CRT Controller.

The microprocessor accesses 19 registers (1 Address and 18 Data Registers) within the C6845 to provide video timing, refresh memory addresses, cursor, and light pen strobe signals. CRT video timing signals include Vertical Sync (VS), Horizontal Sync (HS), and Display Enable (DE) output signals. Refresh memory addressing includes Memory Address (MA[13:0]) and Row Address (RA[4:0]) output buses.

The C6845 microprocessor interface consists of unidirectional data input (DIN[7:0]) and data output (DOUT[7:0]) buses and control signals RS, RWn, CSn, and E. Optionally, an available bus wrapper converts the unidirectional data buses into an 8-bit bidirectional data bus (D[7:0]). This is the pin equivalent to the MC6845.

Functional Description

The C6845 blocks are shown in Figure 1 and described, by sections, below.

Horizontal Timing

The Horizontal Timing section consists of the Horizontal Counter, Horizontal Sync Width Counter, Registers R0 through R3, and associated synchronous Set/Reset Flip-Flops and Coincidence Circuits.

The Horizontal Counter counts from zero until coincidence with Register R0 synchronously resets the counter. This

represents the horizontal line rate and enabling of the Display Enable (DE) for a new line takes place.

Coincidence of the Horizontal Counter with Register R1 marks the end of the Active display portion of a horizontal line with Display Enable (DE) going inactive.

Coincidence of the Horizontal Counter with Register R2 marks the beginning of horizontal retrace with Horizontal Sync (HS) going Active High.

Coincidence of the Horizontal Sync Width Counter with Register R3 marks the end of horizontal retrace with Horizontal Sync (HS) going Inactive Low.

Vertical Timing

The Vertical Timing section consists of the Scan Line Counter, Character Row Counter, Registers R4 through R9, the Vertical Control logic block, and associated Coincidence Circuits.

The Scan Line Counter counts from zero until coincidence with Register R9 synchronously resets the Scan Line Counter and synchronously increments the Character Row Counter. The Scan Line Counter counts the Scan Lines composing a character row, and the Character Row Counter counts the character rows comprising a vertical frame.

The Character Row Counter coincidence with R4 and the residual Scan Line count represented by R5 marks the end of a vertical frame.

The Character Row Counter coincidence with Register R6 marks the end of the Active display portion of the vertical frame measured in character rows.

The Character Row Counter coincidence with Register R7 marks the beginning of vertical retrace with Vertical Sync (VS) going Active High. VS remains High for a fixed period of 16 scan lines.

Register R8, Interlace Mode Register, effects the Vertical Timing according to its programming. Normal Sync (Non-Interlace) mode displays the same field each frame. Interlace Sync Mode splits a frame into even and odd fields. Vertical Sync (VS) Active High is delayed one-half scan line at the end of even fields. For Interlace Sync and Video Mode, in addition to the VS delay on even fields, the Row Address counter sequences on even fields through 0,2,4,… counter values while on odd fields, through 1,3,5,… counter values.

Cursor

The Cursor section consists of the Cursor Control, Cursor Start Register R10, Cursor End Register R11, Cursor Address Registers R14 and R15, and associated Interlace Mode Register settings and Refresh Memory Address and Row Address buses as well as associated Coincidence Circuits.

As a first condition for activating the cursor, Cursor Address Registers R14 and R15 signify the character in linear address space the cursor can be Active. Then, Cursor Start Register R10 and Cursor End Register R11 select the scan lines within the designated character space the cursor will be Active.

In addition, Cursor Start Register R10 contains a 2-bit field indicating whether the cursor is Active or not, and, if so, whether it should blink or not, and, if blink, at 1/16th or 1/32nd the field rate.

Start Address

Start Address Register R12 and R13 indicate the first address the Linear Address Generator puts on the Refresh Memory Address bus at the start of a vertical frame. Whenever the microprocessor writes to R12 and R13, the Linear Address Generator is updated at the start of the next vertical frame.

Light Pen Register

On the rising edge of the LPSTB input, after synchronization by two CLK cycles, the value of the Refresh Memory Address bus is captured by the Light Pen Registers R16 and R17. These registers are readable by way of the microprocessor interface.

Linear Address Generator

The Linear Address Generator generates the Refresh Memory Address. The Linear Address Generator initializes to the value of the Start Address Registers R12 and R13 at the start of each vertical frame. The Linear Address Generator remains Active during horizontal and vertical retrace, for refresh of dynamic RAMs.

Core Modifications

The VHDL source code version of the C6845 core can be customized to include:

- Embed character ROM generator and video line buffers within core
- Wider refresh Memory Address and Row Address buses
- A glueless Intel, ARM, or DSP (or customer choice) microprocessor interface
- Synertek SY6845E or Hitachi HD6845 slightly different features
- Removal of unused functions

Please contact CAST for any required modifications.

Core Assumptions

The C6845 core is functionally equivalent to the Motorola MC6845. The following features are added to the C6845 to enhance the C6845 over the Motorola device. These fea-

tures are additions to the MC6845 and in no way change the MC6845 functions.

In order to create a core with the same interface, a wrapper is required. When the wrapper is employed, buses DIN[7:0] and DOUT[7:0] and signal PDBTRI are replaced with bi-directional data bus D[7:0]. This is the function and pin equivalent to the Motorola MC6845. Without the wrapper, unidirectional buses DIN[7:0] and DOUT[7:0] and control signal PDBTRI can be brought out directly. A sample wrapper is included in the src directory of the C6845 delivery.

The C6845 core contains the input signal PU_RESETn which is not in the Motorola MC6845. According to the MC6845 specification, RESETn and LPSTB reset the MC6845 synchronously with the clock input CLK falling edge. However, the control registers are not affected.

PU_RESETn resets the C6845 asynchronously. The CLK does not have to be Active. In addition, all control registers are reset when PU_RESETn is Active Low (logic “0”). This signal can be used to hard reset the C6845 when the printed circuit board, ASIC, or FPGA has to be reset to a known initial state (and not containing the last values programmed into the C6845 control registers).

If desired, the input signal PU_RESETn can be ignored by pulling up to VCC or removed from the RTL source code.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Verification Methods

The C6845 core’s functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Motorola MC6845 chip, and the results compared with the core’s simulation outputs.

Pin Description

The core signal names are shown in Figure 1 and described in Table 2.

Table 2: Core Signal Pinout

Signal Name	Signal Direction	Description
Microprocessor Interface		
DIN[7..0]	Input	Data Bus Input
DOUT[7..0]	Output	Data Bus Output
PDBTRI	Output	Processor Data Bus Tri-state Control H= Processor Reads L= Processor Writes
RS	Input	Address Register Select
		Data Register Select
RWn	Input	Write to Internal Register
		Read Internal Register
CSn	Input	Chip Select
E	Input	Enable Data Bus Output During Microprocessor Reads (High level)
		Register Data during micro-processor Writes (falling edge)
Light Pen Strobe Interface		
LPSTB	Input	Light Pen Strobe
Reset and Clock Interface		
RESETn	Input	Reset/Test Mode
CLK	Input	Synchronous Clock (Except for Micro-processor Interface)
PU_RESETn	Input	Asynchronous Power-up Reset
CRT Control Interface		
DE	Output	Display Enable
HS	Output	Horizontal Sync
VS	Output	Vertical Sync
Refresh Memory/Character Generator Addressing Interface		
MA[13..0]	Output	Refresh Memory Address
RA[4..0]	Output	Row Address
Cursor Interface		
CURSOR	Output	Cursor

Ordering Information

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Please contact CAST, Inc., for pricing and additional information about this AllianceCORE product.

Related Information

The C6845 core is licensed from Digital Blocks, Inc.

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